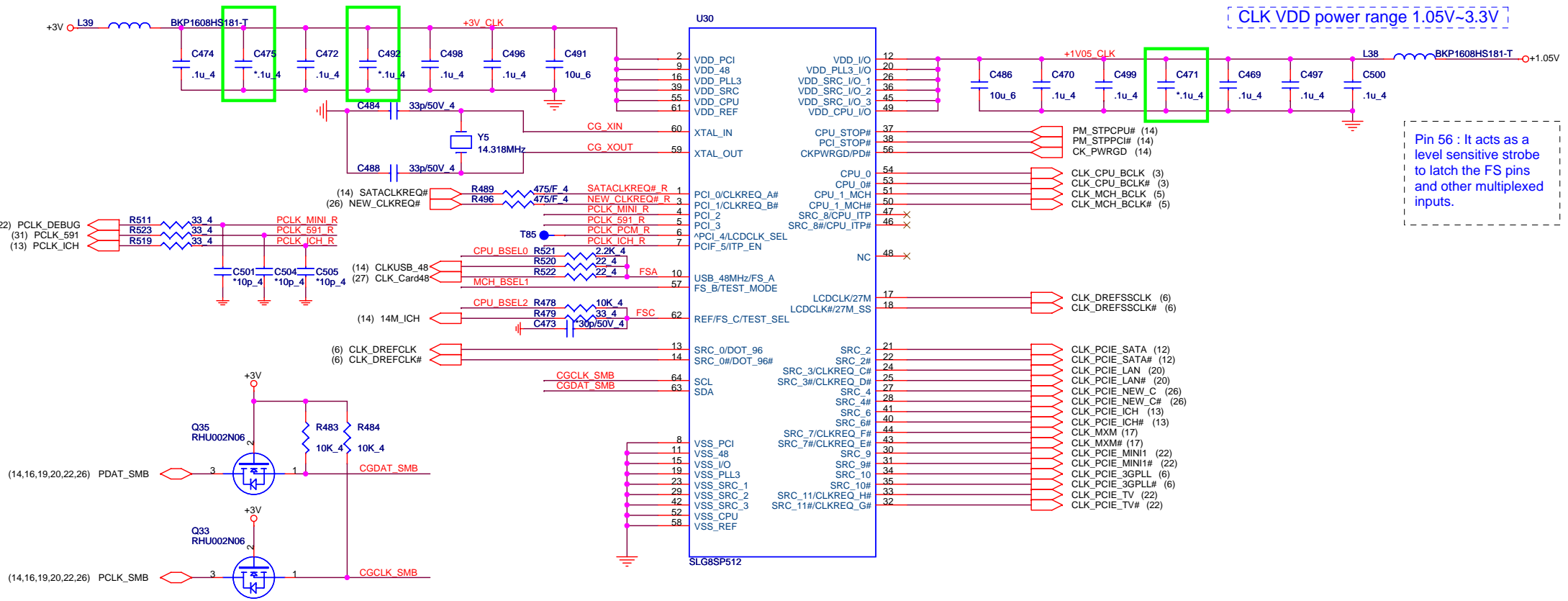


Clock Generator

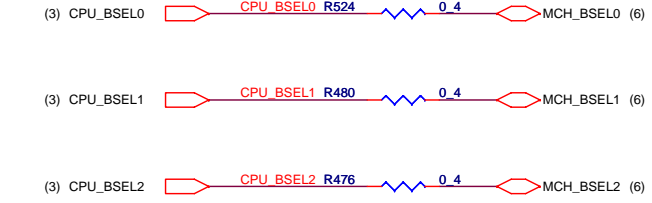


CLK VDD power range 1.05V~3.3V

Pin 56 : It acts as a level sensitive strobe to latch the FS pins and other multiplexed inputs.

CPU Clock select

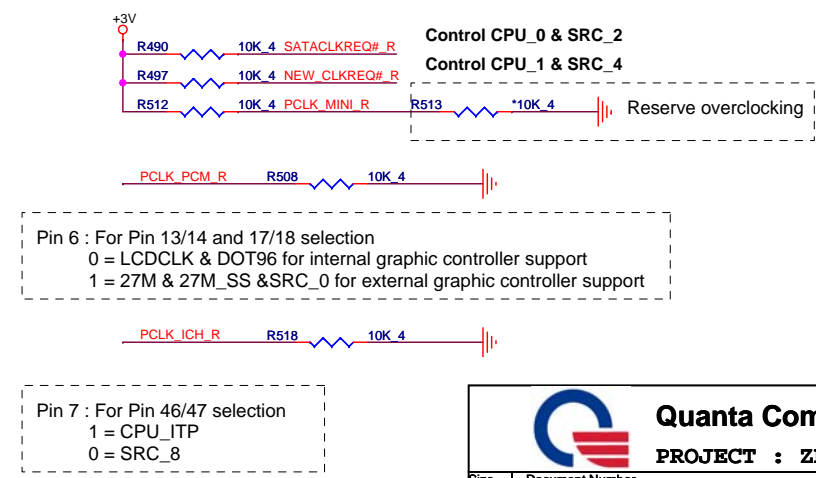
Pin 10/57/62 : For Pin CPU frequency selection

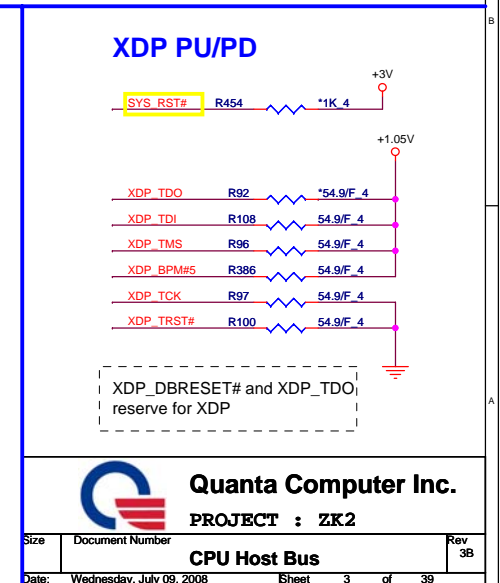
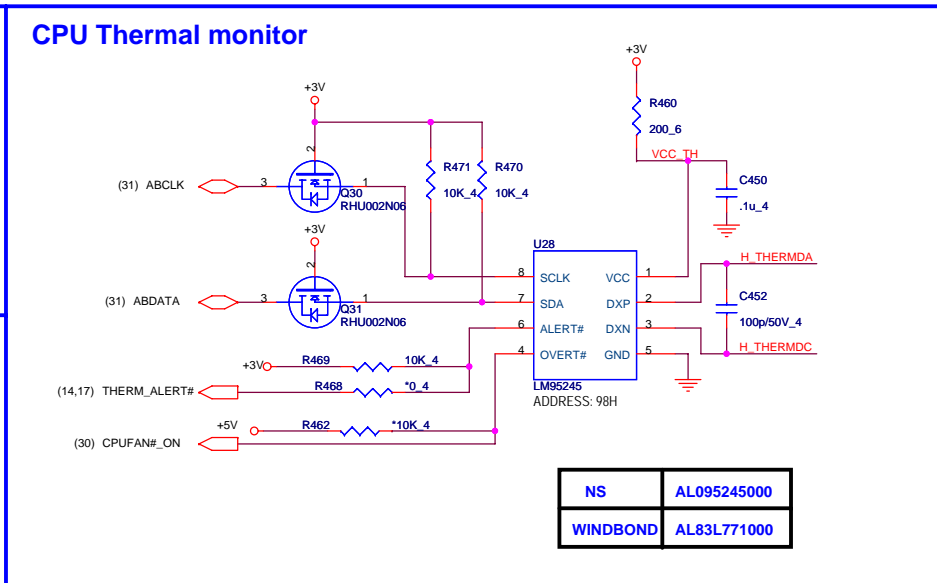
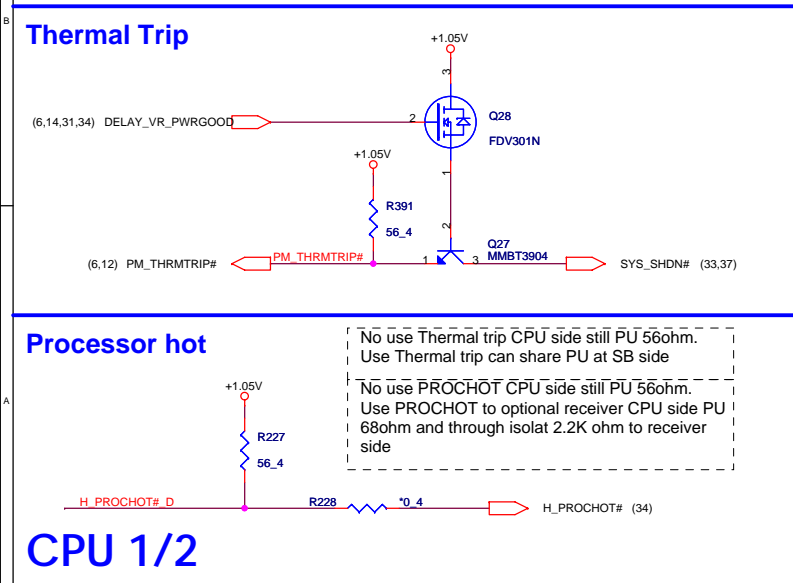
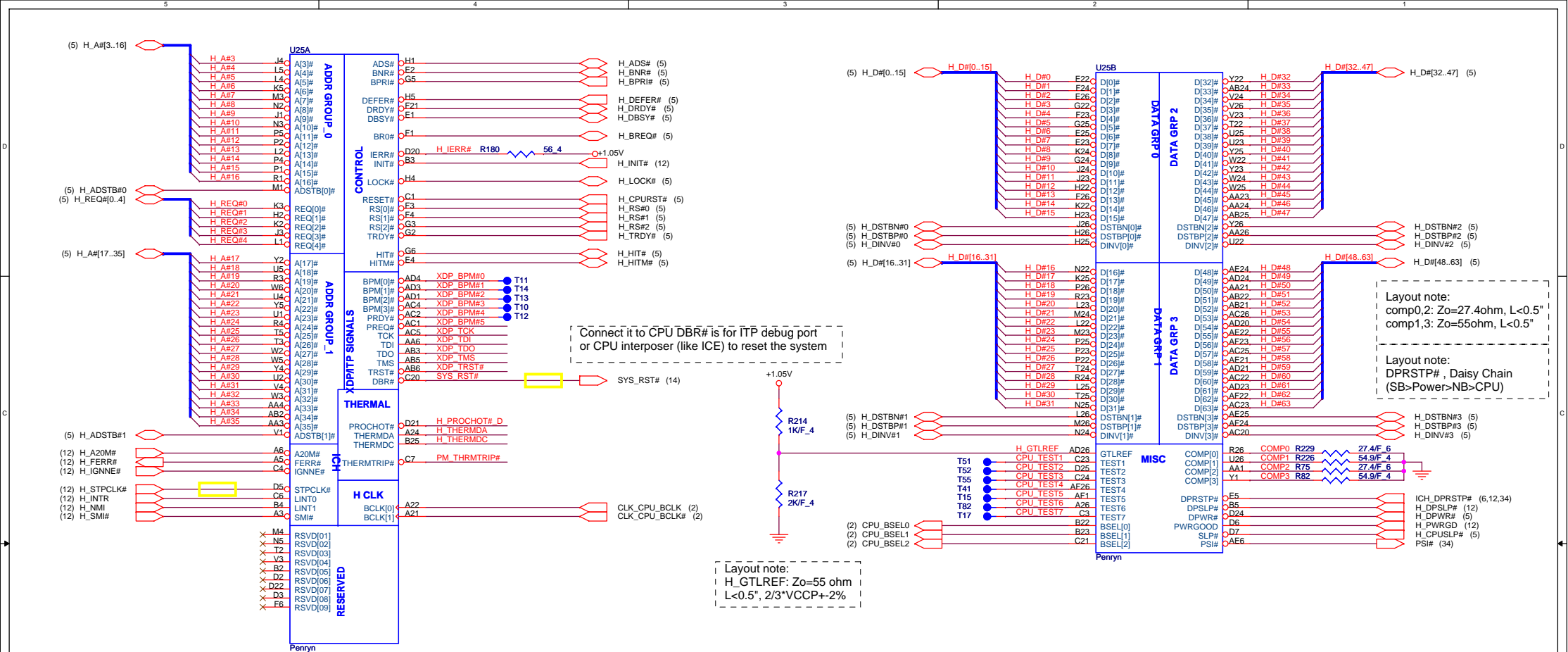


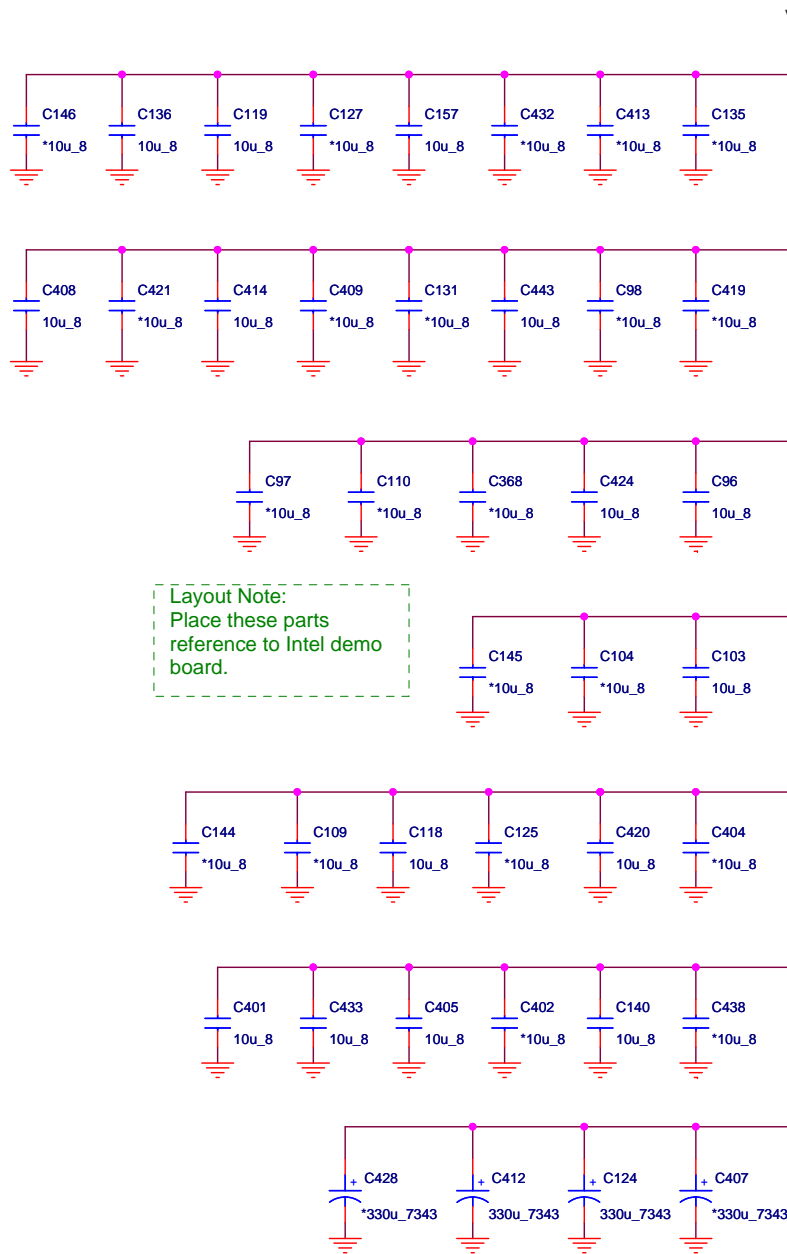
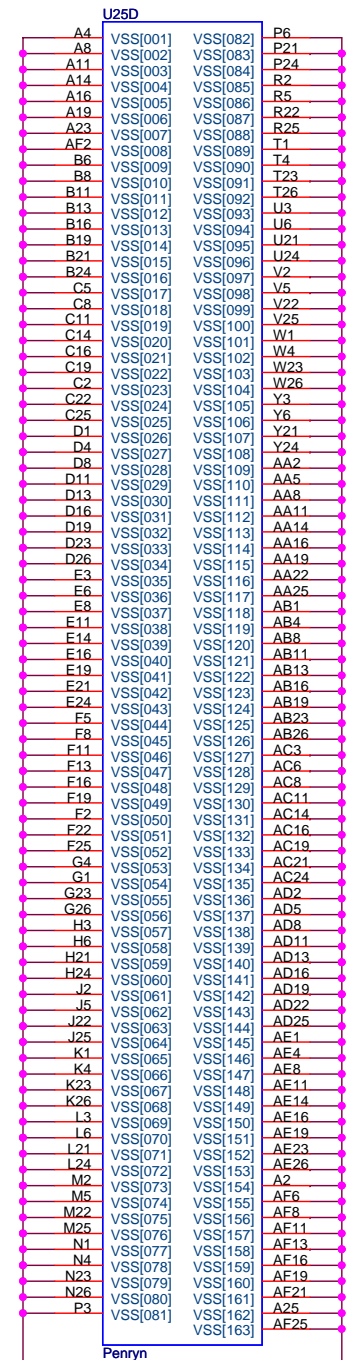
BSEL Frequency Select Table

FSC	FSB	FSA	Frequency
0	0	0	266Mhz
0	0	1	133Mhz
0	1	1	166Mhz
0	1	0	200Mhz
1	1	0	400Mhz
1	1	1	Reserved
1	0	1	100Mhz
1	0	0	333Mhz

Strap table





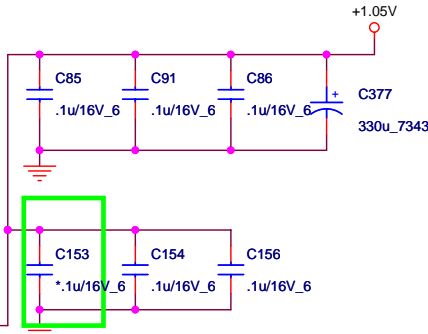


Layout Note:
Place these parts
reference to Intel demo
board.

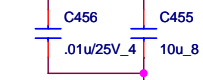
VCC:38A (Low power type)
VCC:47A (Standard type)

Layout Note:
Inside CPU center cavity in 2 rows

VCCP : 2.5A(Supply after VCC Stable)
4.5A(Supply before VCC Stable)



VCCA:130mA



Layout Note:
Z0=27.4,Pu/PD L<1"

Montevina platform : Early Reference Board Schematics Feb 2007. Rev 1.0
stuff 22U*34, NC 22U*2
stuff 330U*2, NC330U*2



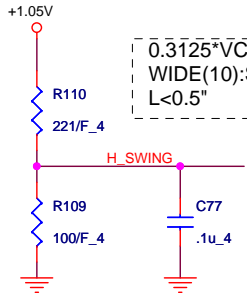
Quanta Computer Inc.
PROJECT : ZK2

Size	Document Number	Rev
		3B
CPU Power		
Date:	Friday, June 27, 2008	Sheet 4 of 39

CPU 2/2

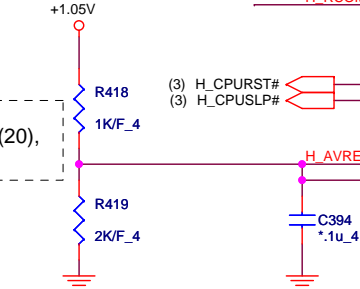
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	QCI P/N
Intel Cantiga (G)M	AJSLB940T04
Intel Cantiga (P)M	AJSLB970T06



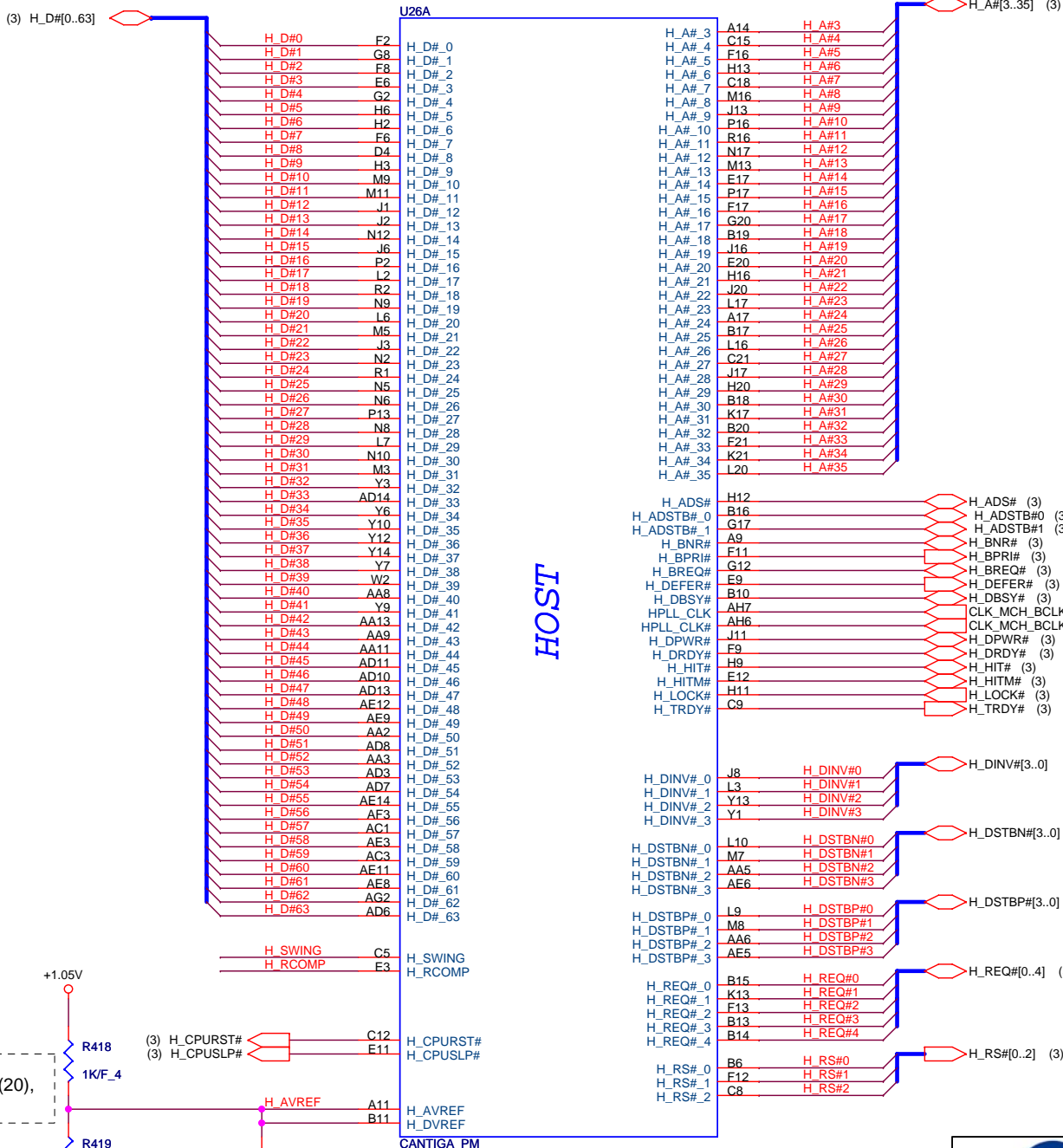
0.3125*VCCP
WIDE(10):SPACING(20) ,
L<0.5"


Layout Note:
WIDE(10):SPACING(20) ,
L<0.5"



2/3*VCCP
WIDE(10):SPACING(20),
L<0.5"

GMCH (CANTIGA)





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PROJECT : ZK2

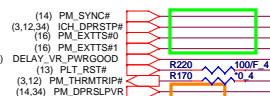
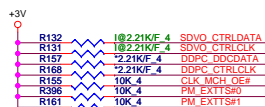
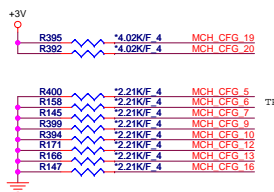
GMCH HOST

Size	Document Number	Rev
		3B
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Strap table

Pin Name	Strap description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB 1066MHz 010 = FSB 800MHz 011 = FSB 667MHz
CFG[4:3]	Reserved	
CFG5	DMI X2 Select	0 = DMI X2 1 = DMI X4(Default)
CFG6	iTPM Host Interface	0 = iTPM Host Interface is enabled 1 = iTPM Host Interface is disabled(Default)
CFG7	ME TLS Confidentiality	0 = AMT Firmware will use TLS cipher suite with no confidentiality 1 = AMT Firmware will use TLS cipher suite with confidentiality(Default)
CFG8	Reserved	
CFG9	PCIe Graphics Lane Reversal	0 = Reverse Lanes 1 = Normal operation(Default)
CFG10	PCIe Loopback enable	0 = Enabled 1 = Disabled (Default)
CFG11	Reserved	
CFG12	ALLZ	0 = ALLZ mode enable 1 = disable(Default)
CFG13	XOR	0 = XOR mode enable 1 = disable(Default)
CFG[15:14]	Reserved	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT disable 1 = Dynamic ODT Enable(Default)
CFG[18:17]	Reserved	
CFG19	DMI Lane Reversal	0 = Normal (Default) 1 = Lanes Reversed
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIe	0 = Only Digital Display port (SDVO/DP/iHDMI) or PCIe is operational (Default) 1 = Digital Display port (SDVO/DP/iHDMI) and PCIe are operating simultaneously via PEG port
SDVO_CTRLDATA	SDVO Present	0 = No SDVO/HDMI Device Present(Default) 1 = SDVO/HDMI Device present
DDPC_CTRLDATA	Digital Display Present	0 = Digital display(HDMI/DP) device absent(Default) 1 = Digital display(HDMI/DP) device present

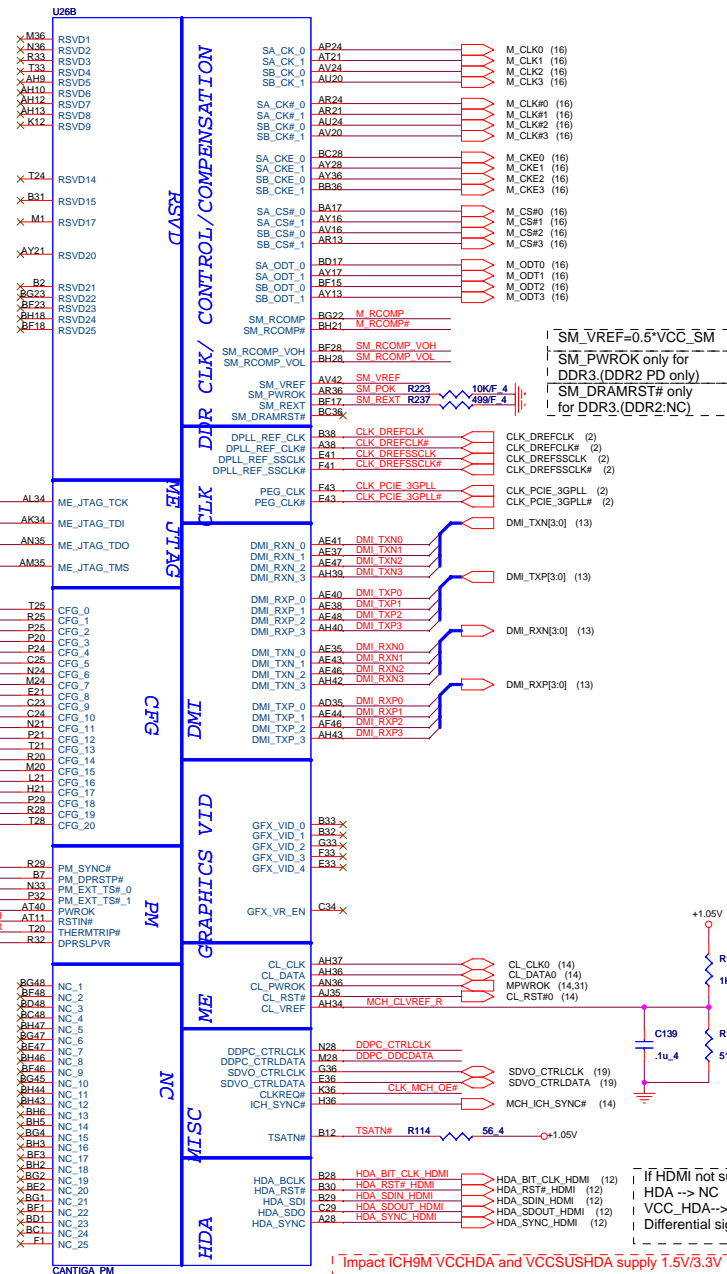
Strap pin



☐ NB Thermal trip pin

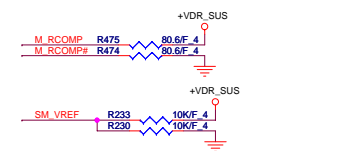
☐ No use Thermal trip NB side can

PM_DPRSTP#
The Daisy chain topology should be routed from ICH9M to IMVP , then to (G)MCH and CPU, in that order.



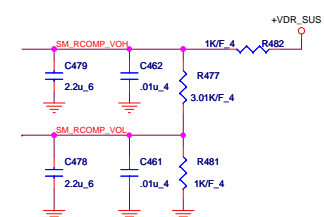
Impact ICH9M VCC_HDA and VCC_SLISHDA supply 1.5V/3

NOTE:
If (G)MCH's HD Audio signals are connected to ICH9M for iHDMI, VCCHDA and VCCSUSDA on ICH9M should be only on 1.5V. These power pins on ICH9M can be supplied with 3.3V if and only if (G)MCH's HDA is not connected to ICH9M. Consequently, only 1.5V audio/modem codecs can be used on the platform.

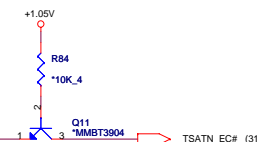


SM_VREF.Default use voltage divider for poor layout cause +SMDDR_VREF not meet spec.And Intel circuit PU/PD is 1K.But Check list PU/PD is 10K.

INTEL FAE Suggest PD for Ext graphics



NB Thermaltrip



Check list note : CL_VREF=0.35V

```
DDPC_CTRL for HDMI port C
SDVO_CTRL for HDMI port B
```

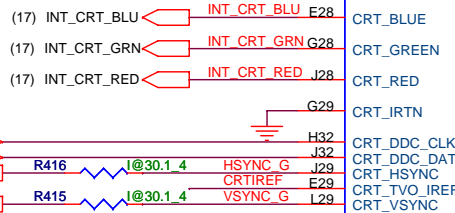
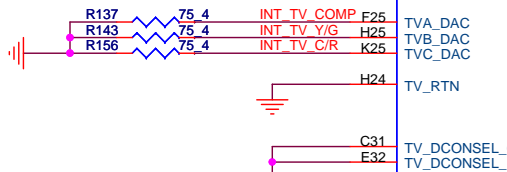
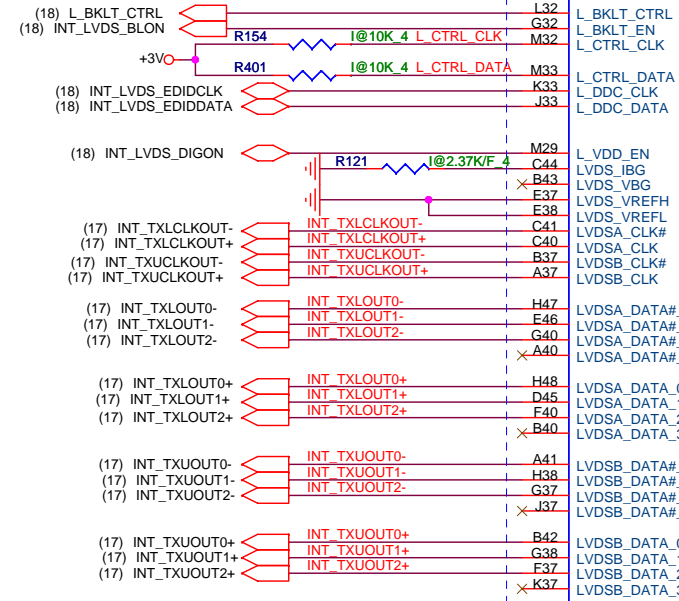
<Checklist ver0.8>
If TSATN# is not used, then it must be terminated with a 56-Ω pull-up resistor to VCCP.

- ! <Pin out check issue>

IV@
EV@
SP@

IV&EV Dis/Enable setting

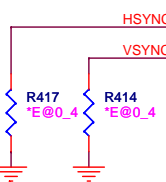
If LVDS no use,all signal can NC



HSYNC/VSYNC serial R place close to NB

CRTIREF pull down for IV cantiga 1.02k ohm/F

MXM STUFFED.



L<0.5", If PCIE not support still connect to +VCC_PEG

PEG_COMPI
PEG_COMPO

PEG_RX#_0
PEG_RX#_1
PEG_RX#_2
PEG_RX#_3
PEG_RX#_4
PEG_RX#_5
PEG_RX#_6
PEG_RX#_7
PEG_RX#_8
PEG_RX#_9
PEG_RX#_10
PEG_RX#_11
PEG_RX#_12
PEG_RX#_13
PEG_RX#_14
PEG_RX#_15

PEG_RX_0
PEG_RX_1
PEG_RX_2
PEG_RX_3
PEG_RX_4
PEG_RX_5
PEG_RX_6
PEG_RX_7
PEG_RX_8
PEG_RX_9
PEG_RX_10
PEG_RX_11
PEG_RX_12
PEG_RX_13
PEG_RX_14
PEG_RX_15

PEG_TX#_0
PEG_TX#_1
PEG_TX#_2
PEG_TX#_3
PEG_TX#_4
PEG_TX#_5
PEG_TX#_6
PEG_TX#_7
PEG_TX#_8
PEG_TX#_9
PEG_TX#_10
PEG_TX#_11
PEG_TX#_12
PEG_TX#_13
PEG_TX#_14
PEG_TX#_15

PEG_TX_0
PEG_TX_1
PEG_TX_2
PEG_TX_3
PEG_TX_4
PEG_TX_5
PEG_TX_6
PEG_TX_7
PEG_TX_8
PEG_TX_9
PEG_TX_10
PEG_TX_11
PEG_TX_12
PEG_TX_13
PEG_TX_14
PEG_TX_15

H44 PEG RXN0
J46 PEG RXN1
L44 PEG RXN2
L40 PEG RXN3
N41 PEG RXN4
P48 PEG RXN5
N44 PEG RXN6
T43 PEG RXN7
U43 PEG RXN8
Y43 PEG RXN9
Y48 PEG RXN10
Y36 PEG RXN11
AA43 PEG RXN12
AD37 PEG RXN13
AC47 PEG RXN14
AD39 PEG RXN15

H43 PEG RXP0
J44 PEG RXP1
L43 PEG RXP2
L41 PEG RXP3
N40 PEG RXP4
P47 PEG RXP5
N43 PEG RXP6
T42 PEG RXP7
U42 PEG RXP8
Y42 PEG RXP9
V47 PEG RXP10
Y37 PEG RXP11
AA42 PEG RXP12
AD36 PEG RXP13
AC48 PEG RXP14
AD40 PEG RXP15

J41 C PEG TXN0 C88
M46 C PEG TXN1 C80
M47 C PEG TXN2 C90
M40 C PEG TXN3 C100
M42 C PEG TXN4 C102
R48 C PEG TXN5 C107
N38 C PEG TXN6 C111
T40 C PEG TXN7 C122
U37 C PEG TXN8 C123
U40 C PEG TXN9 C142
Y40 C PEG TXN10 C152
AA46 C PEG TXN11 C134
AA37 C PEG TXN12 C155
AA40 C PEG TXN13 C176
AD43 C PEG TXN14 C216
AC46 C PEG TXN15 C172

J42 C PEG TXP0 C89
L46 C PEG TXP1 C75
M48 C PEG TXP2 C82
M39 C PEG TXP3 C94
M43 C PEG TXP4 C101
R47 C PEG TXP5 C105
N37 C PEG TXP6 C108
T39 C PEG TXP7 C115
U36 C PEG TXP8 C120
U39 C PEG TXP9 C138
Y38 C PEG TXP10 C151
Y46 C PEG TXP11 C128
AA36 C PEG TXP12 C148
AA39 C PEG TXP13 C175
AD42 C PEG TXP14 C219
AD46 C PEG TXP15 C171

Can support reversal routing.If CFG9=1, PCI Express is normal operation. If CFG9=0, then PEG_TXP0 becomes PEG_TXP15, PEG_TXP1 becomes PEG_TXP14, PEG_TXP2 becomes PEG_TXP13, etc. similarly for PEG_RXP[15:0] and PEG_RXN[15:0]

IV&EV Dis/Enable setting

<5/31>Montevina_Schematics_Checklist_Rev0_8
a)For TVOUT Disabled, TV_DCONSEL[1:0] Connect to GND. But design guide Rev0.7 show NC.What is correct.
b)For CRT DAC Disable, CRT_DDC_CLK, CRT_DDC_DATA, CRT_HSYNC, CRT_VSYNCThese signals should be connected to GND. But design guide Rev0.7 show NC, Intel suggest follow Design guide.

<check list>

For EV@
CRT R/G/B 0ohm to GND
CRTIREF 0ohm to GND

<check list>

For IV@
CRT R/G/B 150ohm to GND
CRTIREF 1.02Kohm to GND

CRTIREF
For IV: 1.02Kohm
For EV:0ohm



CRT_R/G/B
For IV: 150ohm
For EV:0ohm

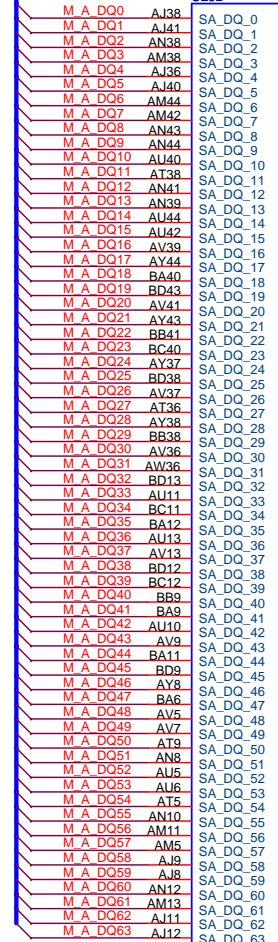


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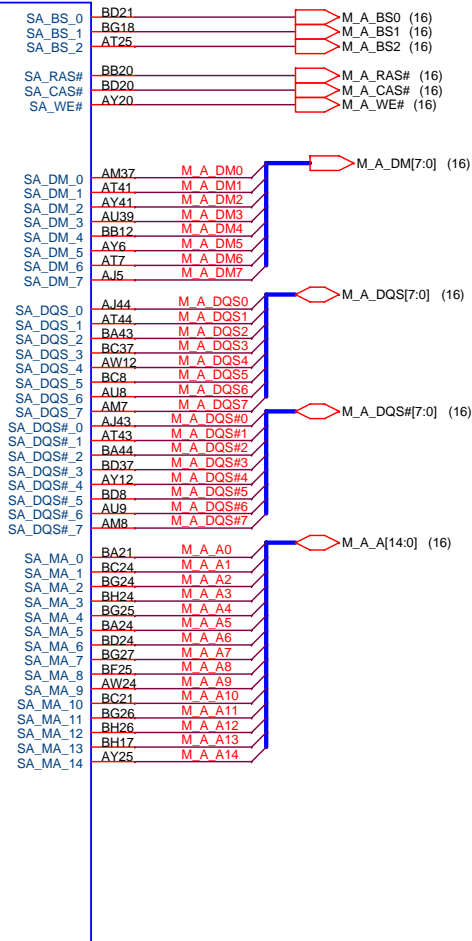
PROJECT : ZK2

GMCH VGA

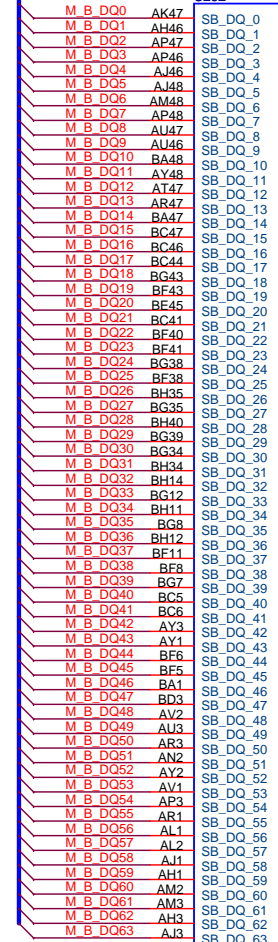
(16) M_A_DQ[63:0]



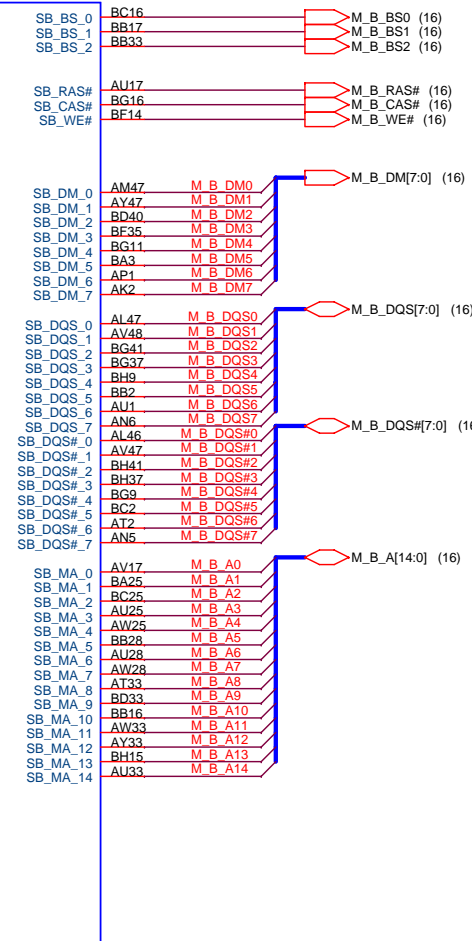
DDR SYSTEM MEMORY A



(16) M_B_DQ[63:0]




DDR SYSTEM MEMORY B



GMCH (CANTIGA)

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PROJECT : ZK2

Size	Document Number	Rev 3B
GMCH DDRII		
Date:	Friday, June 27, 2008	Sheet 8 of 39

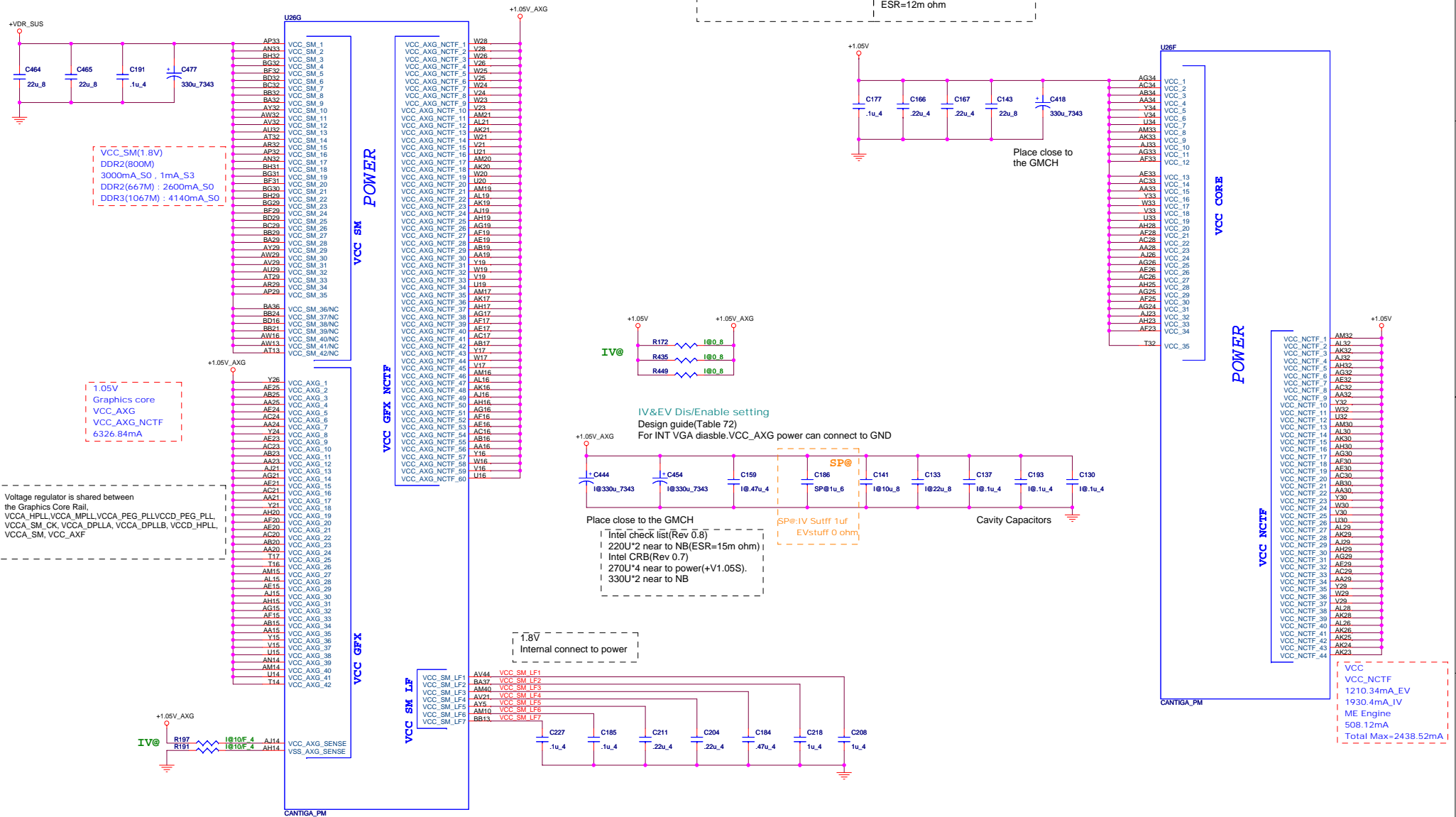
GM	TDP	10.5~12W
GS	TDP	7~8W
PM	TDP	7W

Intel check list(Rev 0.8)
No description for VCC_SM bulk CAP
Intel CRB(Rev 0.7)
330U*1 Reserve near to power
330U*1 near to NB

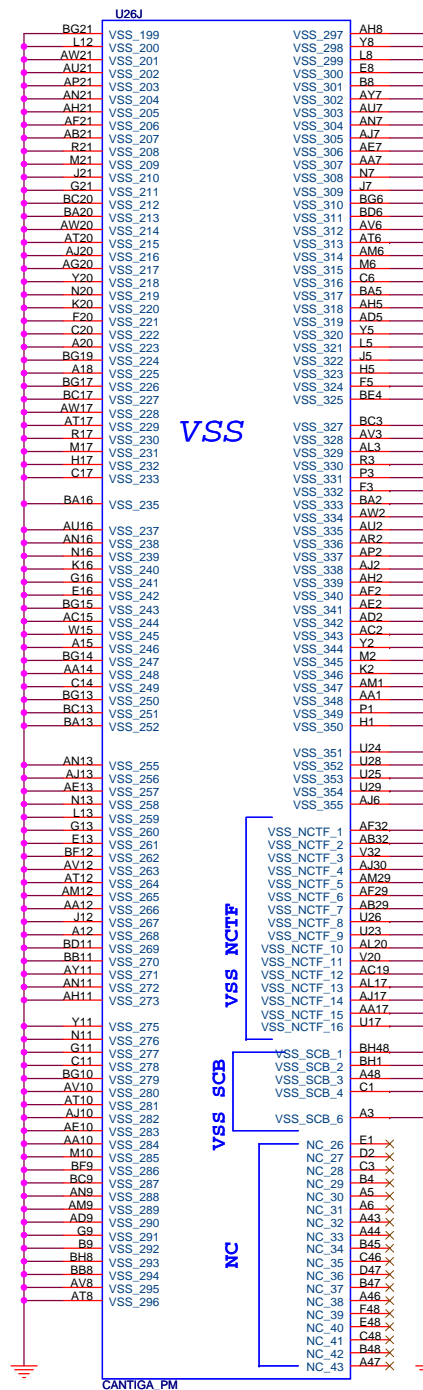
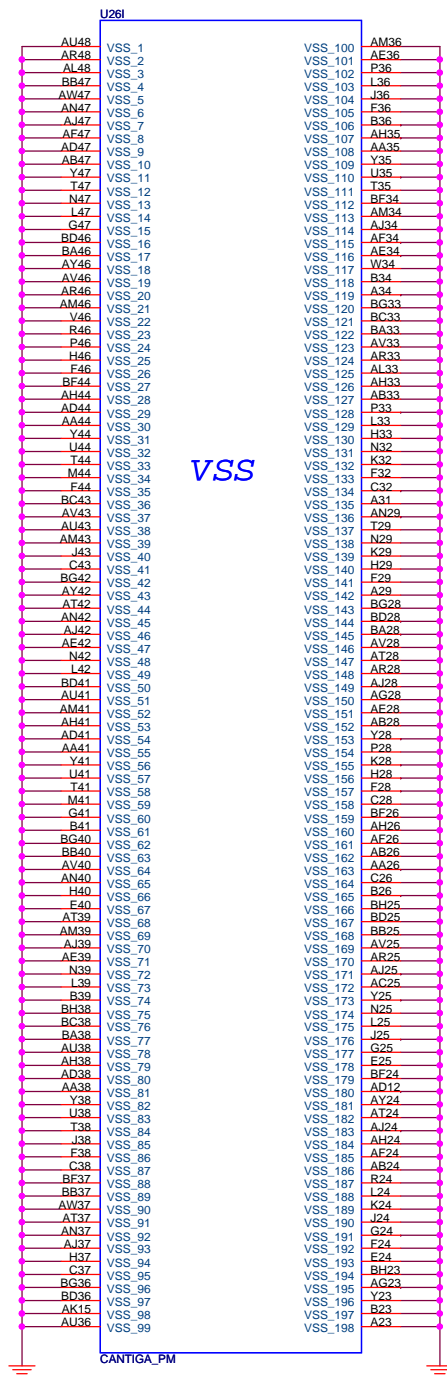
```

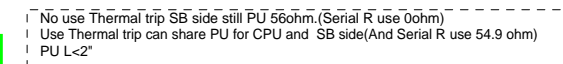
| Intel check list(Rev 0.8)
| 270U*1 near to power(+V1.05M).
| 270U*2 near to NB
| Intel CRB(Rev 0.7)
| 270U*3 near to power(+V1.05M).
| 270U*1 near to NB
| ESR=12m ohm

```

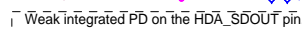


GMCH (CANTIGA)

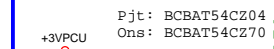




HD Audio



RTC



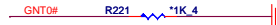



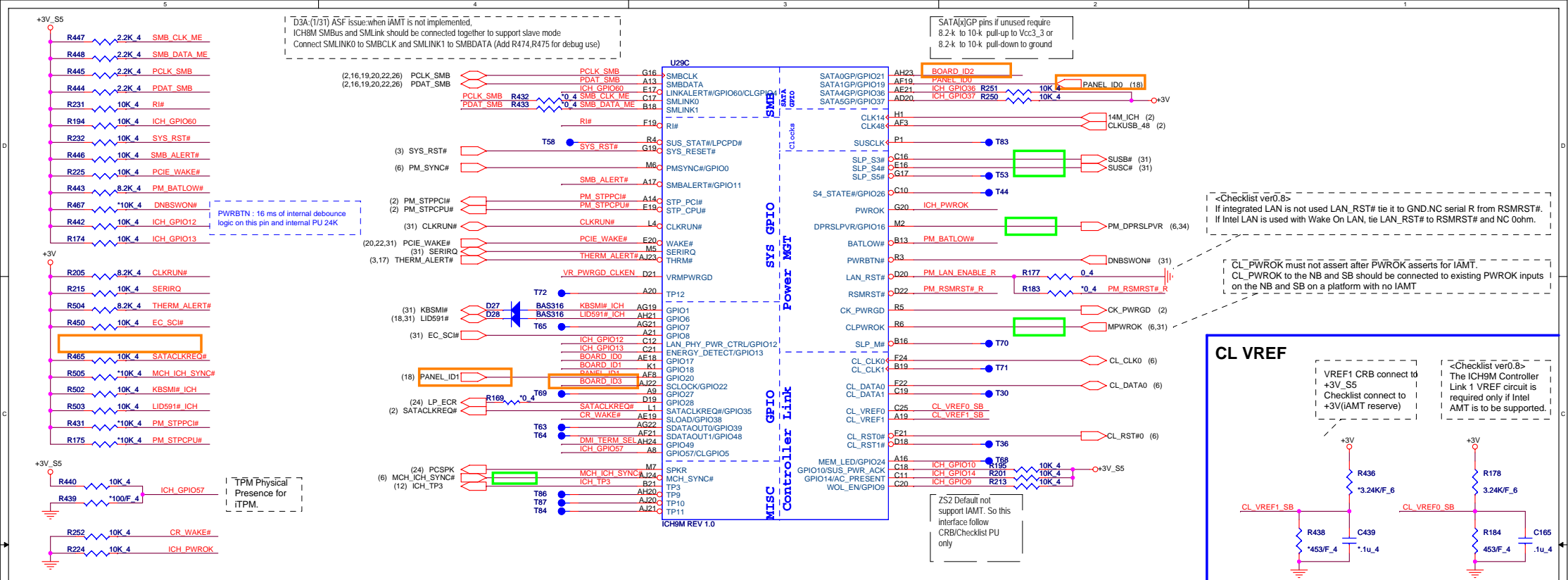
South Bridge Strap Pin (1/3)

(14) ICH_TP3  ICH_TP3 R451  *1K_4 

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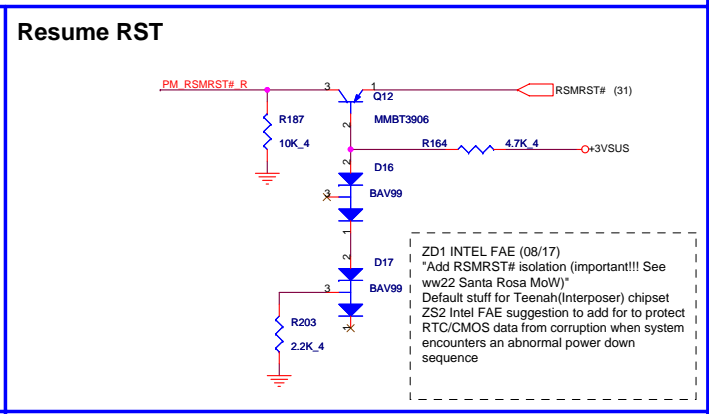
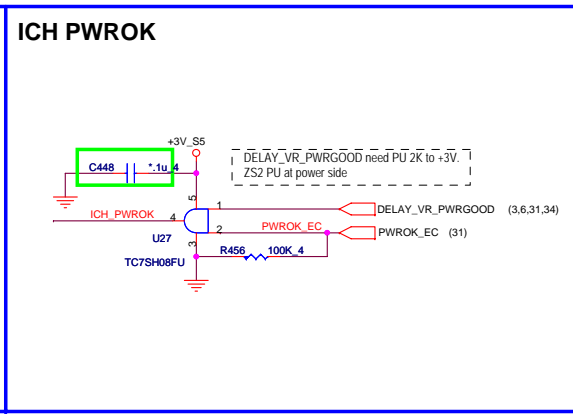
Pin Name	Strap description	Sampled	Configuration	PU/PD		
HDA_SYNC	PCI Express Port Config 1 bit 0 (Port 1-4)	PWROK	0 = Default 1 = Setting bit 0			
GNT2# / GPIO53	PCI Express Port Config 2 bit 2 (Port 5-6)	PWROK	0 = Setting bit 2 1 = Default			
GNT1# / GPIO51	ESI Strap(Server Only)	PWROK	0 = DMI for ESI-compatible 1 = Default			
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default			
SPI_MOSI	Integrated TPM Enable	CLPWROK	0 = INT TPM disable(Default) 1 = INT TPM enable			
GNT0#	Boot BIOS Selection 0	PWROK	PCI_GNT#0	SPI_CS#1	Boot Location	
			0	1	SPI	
SPI_CS1# / GPIO58 / CLGPIO6	Boot BIOS Selection 1	CLPWROK	1	0	PCI	
			1	1	LPC(Default)	



Panel ID (UMA only)

Close to LCD connector (CN3)

P_ID1 (GPIO20)	P_ID0 (GPIO19)	Resolution
0	0	1366x768
0	1	1920x1080
1	0	Reserved
1	1	Reserved

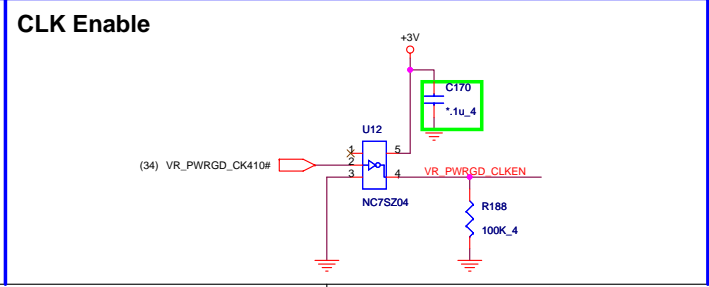


M/B ID

Board ID	ID3	ID2	ID1	ID0
default	0	0	0	0
	0	0	0	1
	0	0	1	0
	0	0	1	1
	0	1	0	0

South Bridge Strap Pin (3/3)

Pin Name	Strap description	Sampled	Configuration	PU/PD
GPIO20	Reserved	PWROK		
SPKR	No Reboot	PWROK	0 = Default 1 = No Reboot mode	PCSPK R236 *1K_4 +3V
GPIO49	DMI Termination Voltage	PWROK	0 = for desktop applications 1 = for mobile applications Internal PU	DMI_TERM_SEL R507 *1K_4



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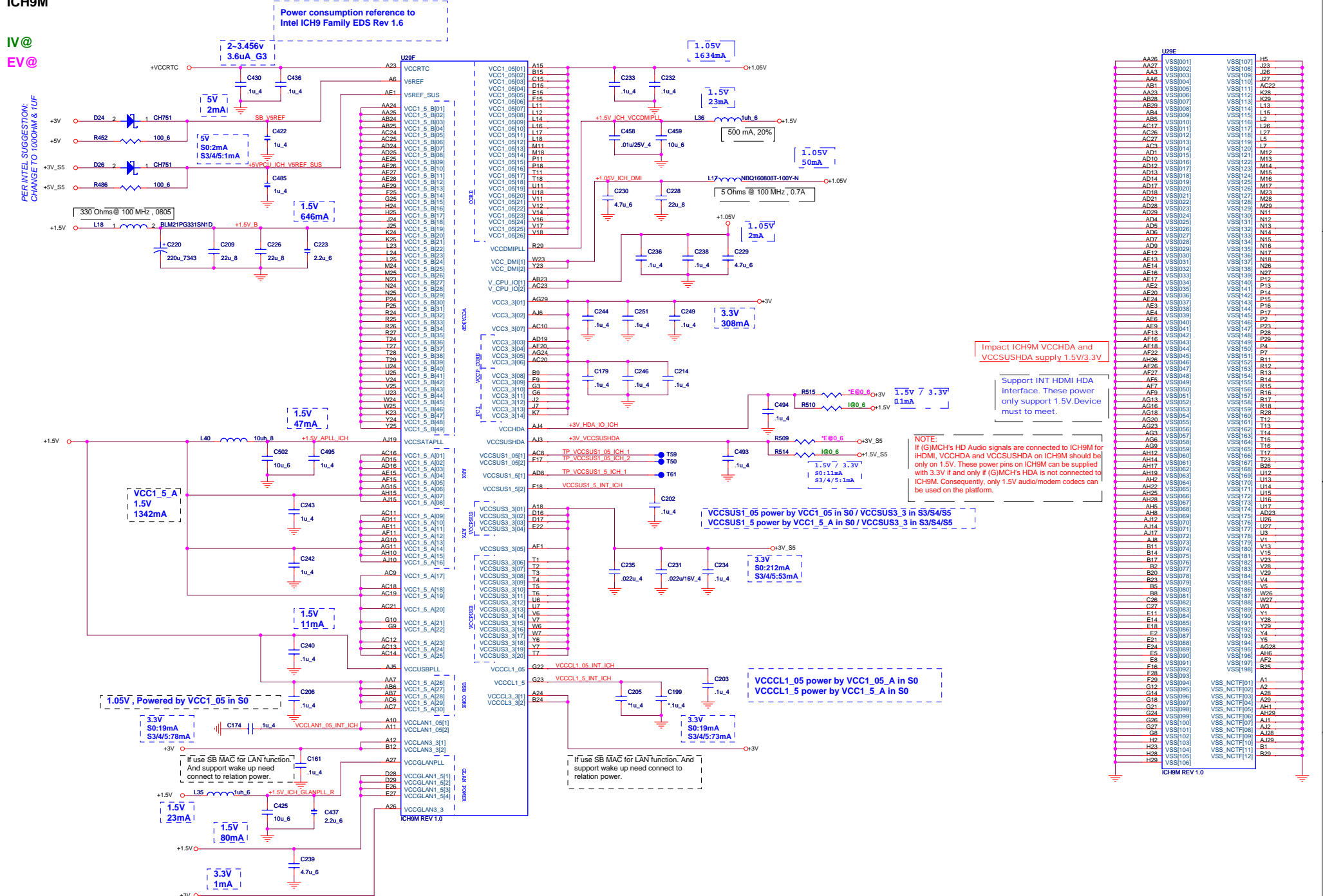
PROJECT : ZK2

ICH9M GPIO

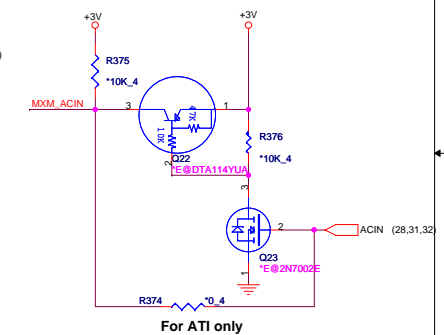
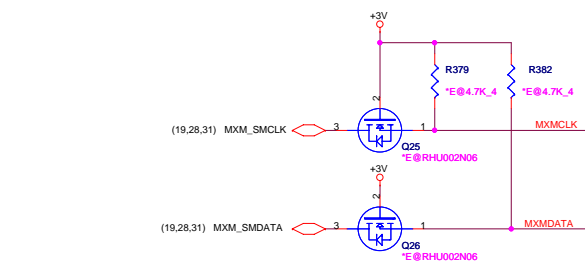
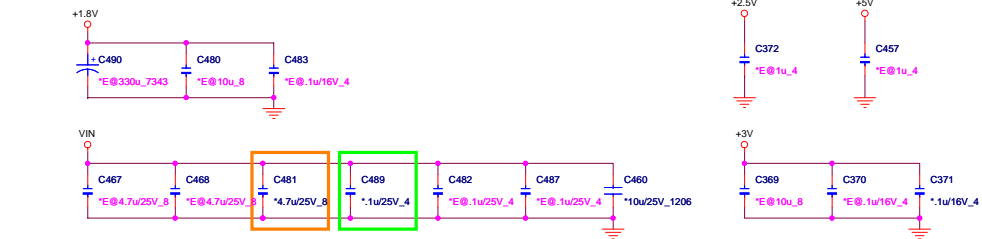
Rev 3B

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IV@
EV@



(18)	VGA_RED	VGA_RED	R104	100.4	INT_CRT_RED	(7)
(18)	VGA_GRN	VGA_GRN	R105	100.4	INT_CRT_GRN	(7)
(18)	VGA_BLU	VGA_BLU	R106	100.4	INT_CRT_BLU	(7)
(18)	HSYNC	HSYNC	R99	100.4	INT_HSYNC	(7)
(18)	VSYNC	VSYNC	R98	100.4	INT_VSYNC	(7)
(18)	CRTDCLK	CRTDCLK	R90	100.4	INT_CRT_DDCCLK	(7)
(18)	CRTDDAT	CRTDDAT	R81	100.4	INT_CRT_DDCDAT	(7)

(18) TXCLKOUT-	TXCLKOUT-	TXCLKOUT+	RN20	3	4	2	I@0.4P2R	INT TXCLKOUT-	INT TXCLKOUT+	INT TXCLKOUT- (7)	INT TXCLKOUT+ (7)
(18) TXCLKOUT+											
(18) TXOUT0-	TXOUT0-	TXOUT0+	RN17	3	4	2	I@0.4P2R	INT TXOUT0-	INT TXOUT0+	INT TXOUT0- (7)	INT TXOUT0+ (7)
(18) TXOUT0+											
(18) TXOUT1-	TXOUT1-	TXOUT1+	RN18	3	4	2	I@0.4P2R	INT TXOUT1-	INT TXOUT1+	INT TXOUT1- (7)	INT TXOUT1+ (7)
(18) TXOUT1+											
(18) TXOUT2-	TXOUT2-	TXOUT2+	RN19	3	4	2	I@0.4P2R	INT TXOUT2-	INT TXOUT2+	INT TXOUT2- (7)	INT TXOUT2+ (7)
(18) TXOUT2+											
(18) TXCLKOUT-	TXCLKOUT-	TXCLKOUT+	RN24	3	4	2	I@0.4P2R	INT TXCLKOUT-	INT TXCLKOUT+	INT TXCLKOUT- (7)	INT TXCLKOUT+ (7)
(18) TXCLKOUT+											
(18) TXOUT0-	TXOUT0-	TXOUT0+	RN21	3	4	2	I@0.4P2R	INT TXOUT0-	INT TXOUT0+	INT TXOUT0- (7)	INT TXOUT0+ (7)
(18) TXOUT0+											
(18) TXOUT1-	TXOUT1-	TXOUT1+	RN22	3	4	2	I@0.4P2R	INT TXOUT1-	INT TXOUT1+	INT TXOUT1- (7)	INT TXOUT1+ (7)
(18) TXOUT1+											
(18) TXOUT2-	TXOUT2-	TXOUT2+	RN23	3	4	2	I@0.4P2R	INT TXOUT2-	INT TXOUT2+	INT TXOUT2- (7)	INT TXOUT2+ (7)
(18) TXOUT2+											

PEG_RXP3 R437 I0_4 TMD5_HDP# (19)

Input	Control	Output
PEG_TXN2 RN7	1	INT_HDMITXN0 (19)
PEG_TXP2	3	INT_HDMITXP0 (19)
PEG_TXN1 RN6	1	INT_HDMITXN1 (19)
PEG_TXP1	3	INT_HDMITXP1 (19)
PEG_TXN0 RN5	1	INT_HDMITXN2 (19)
PEG_TXP0	3	INT_HDMITXP2 (19)
PEG_TXN3 RN8	1	INT_HDMITXN3 (19)
PEG_TXP3	3	INT_HDMITXP3 (19)

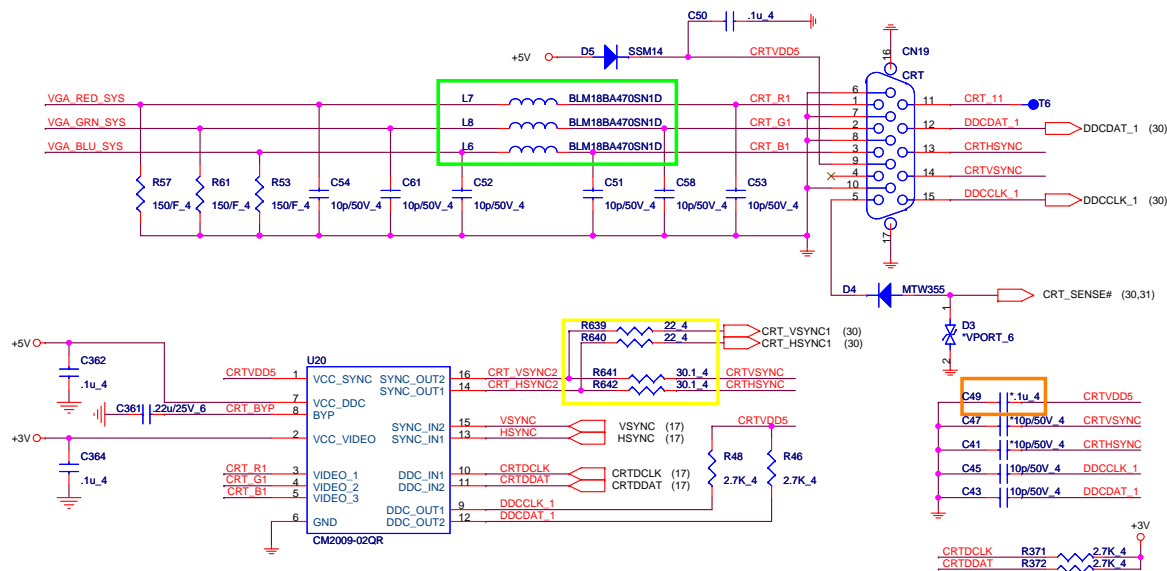
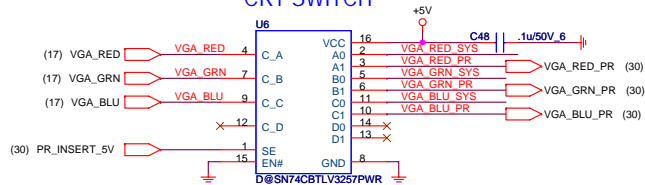


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	MXM	3B
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CRT

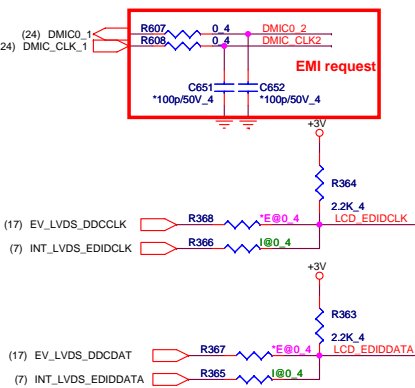
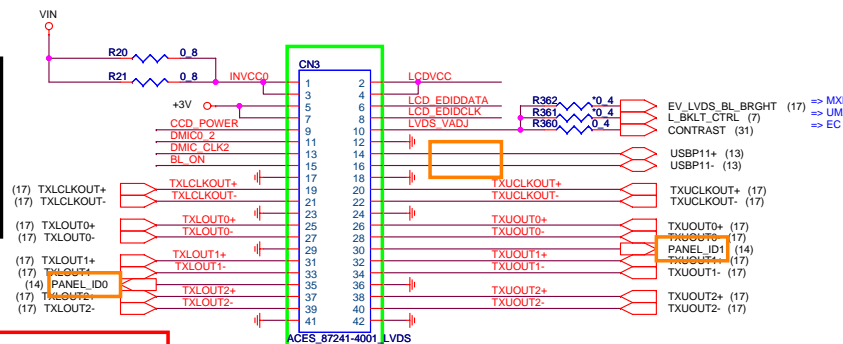
IV@
EV@

CRT SWITCH

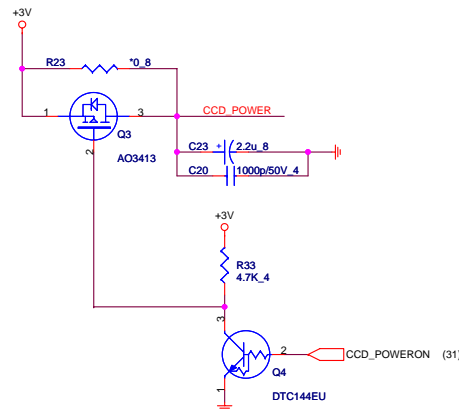


LVDS

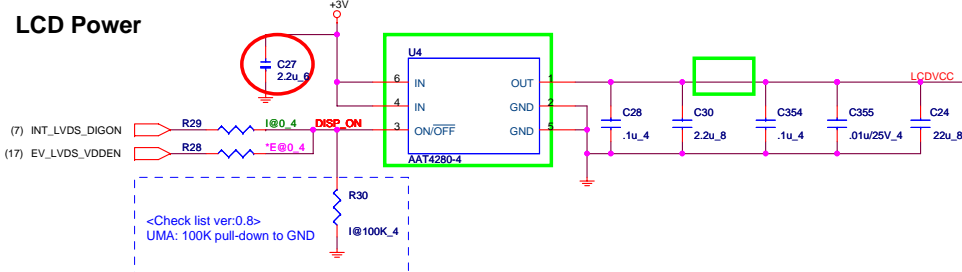
P_ID1	P_ID0	Resolution
0	0	1366x768
0	1	1920x1080
1	0	Reserved
1	1	Reserved



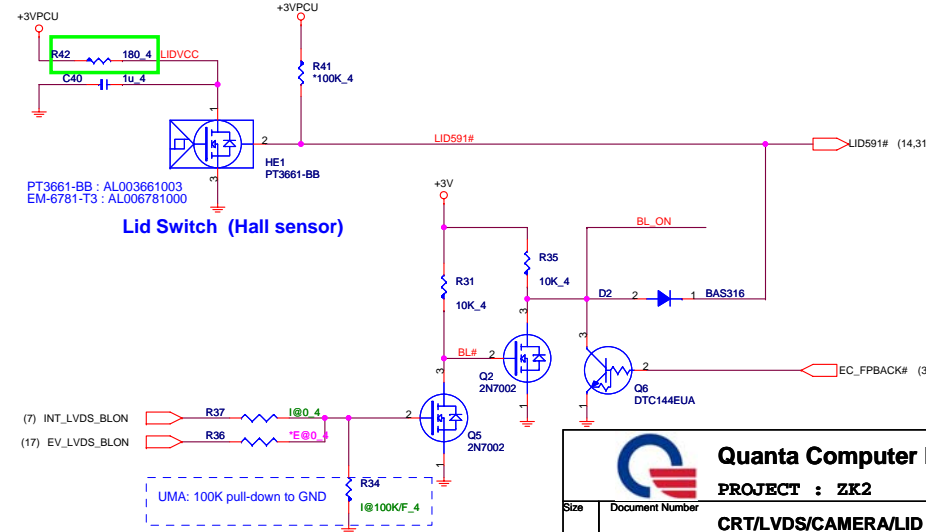
CCD



LCD Power



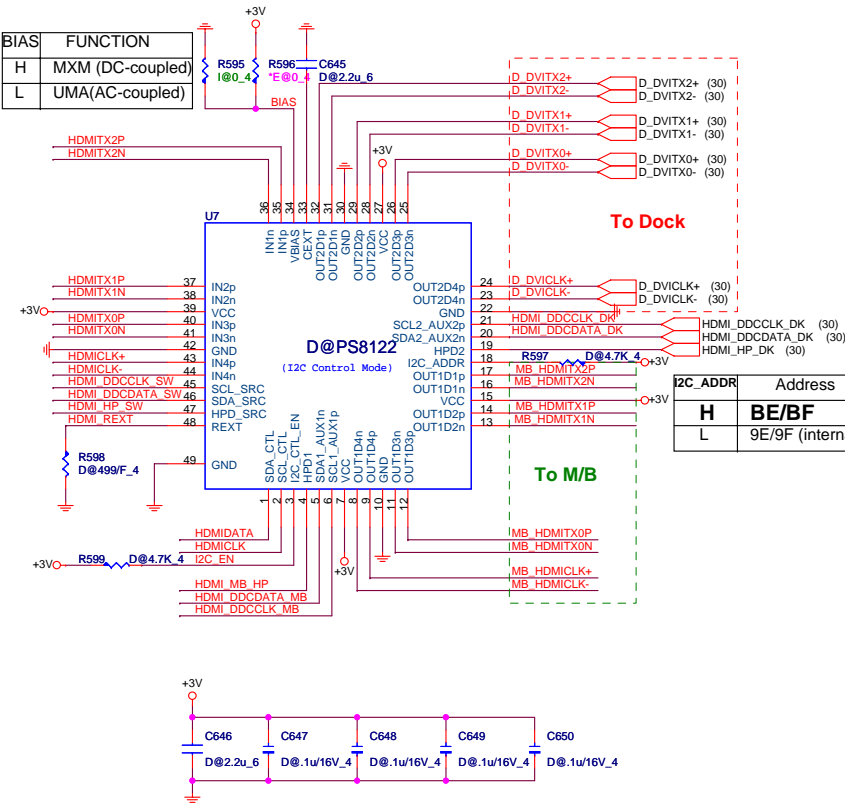
Backlight Control & LID



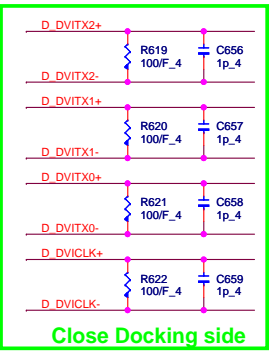
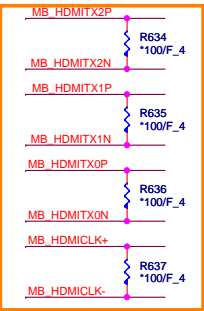
HDMI Switch

IV@
EV@
SP@

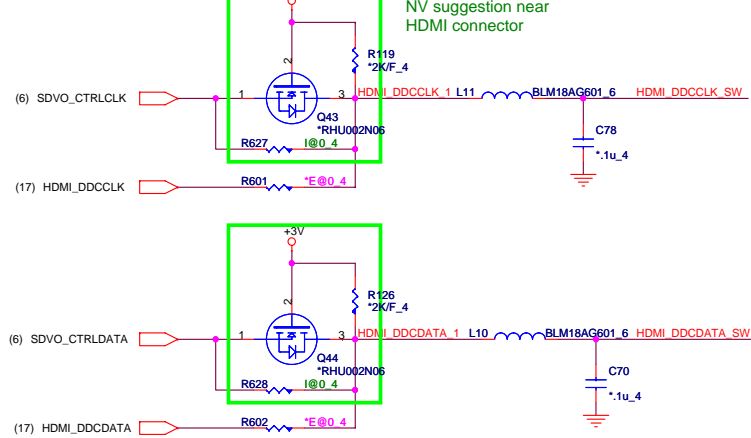
BIAS	FUNCTION
H	MXM (DC-coupled)
L	UMA(AC-coupled)



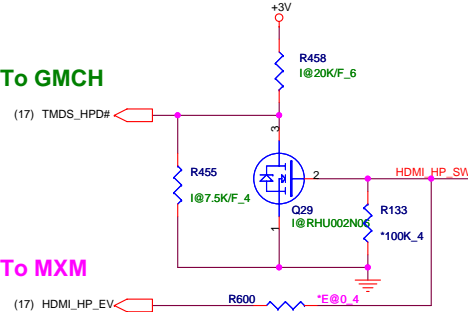
EMI reserve



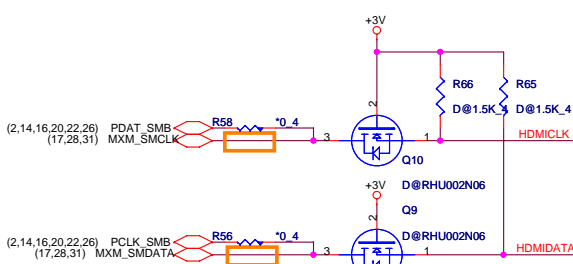
SDVO I2C Control



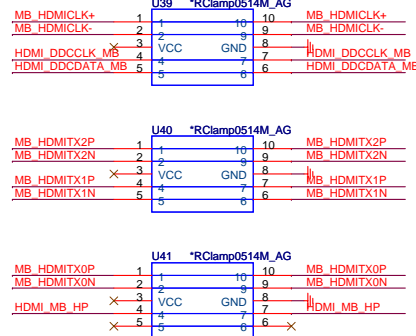
HP-detect



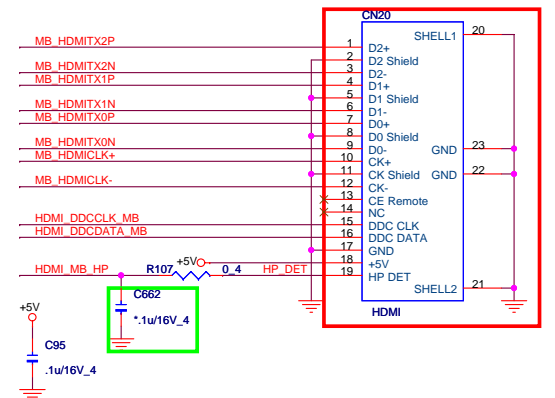
SMBUS



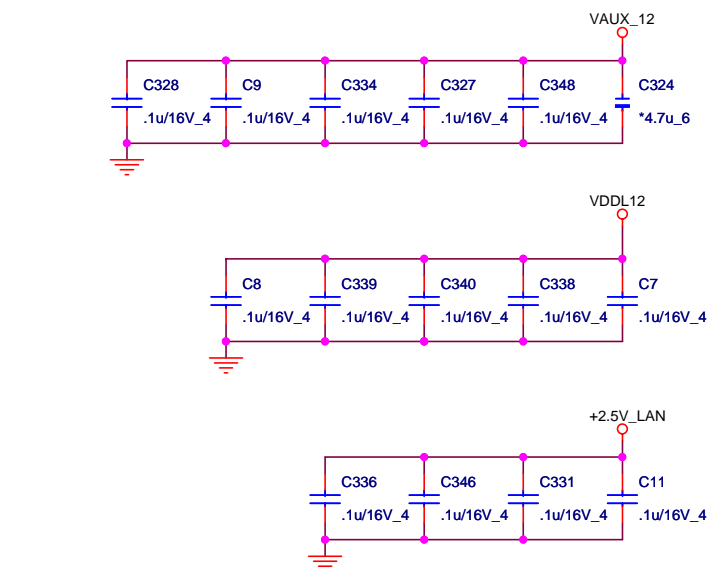
ESD Protect



HDMI connector



Decoupling CAP



PROJECT : ZK2

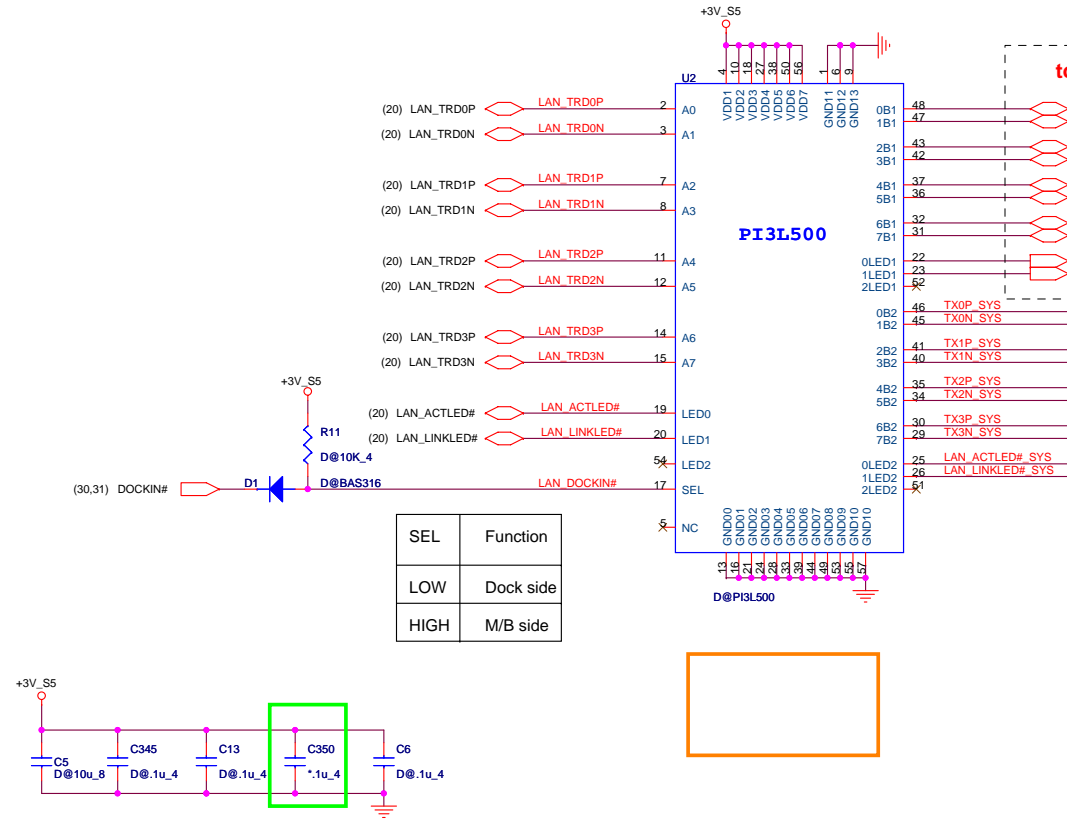
AR8121 LANRev
3B

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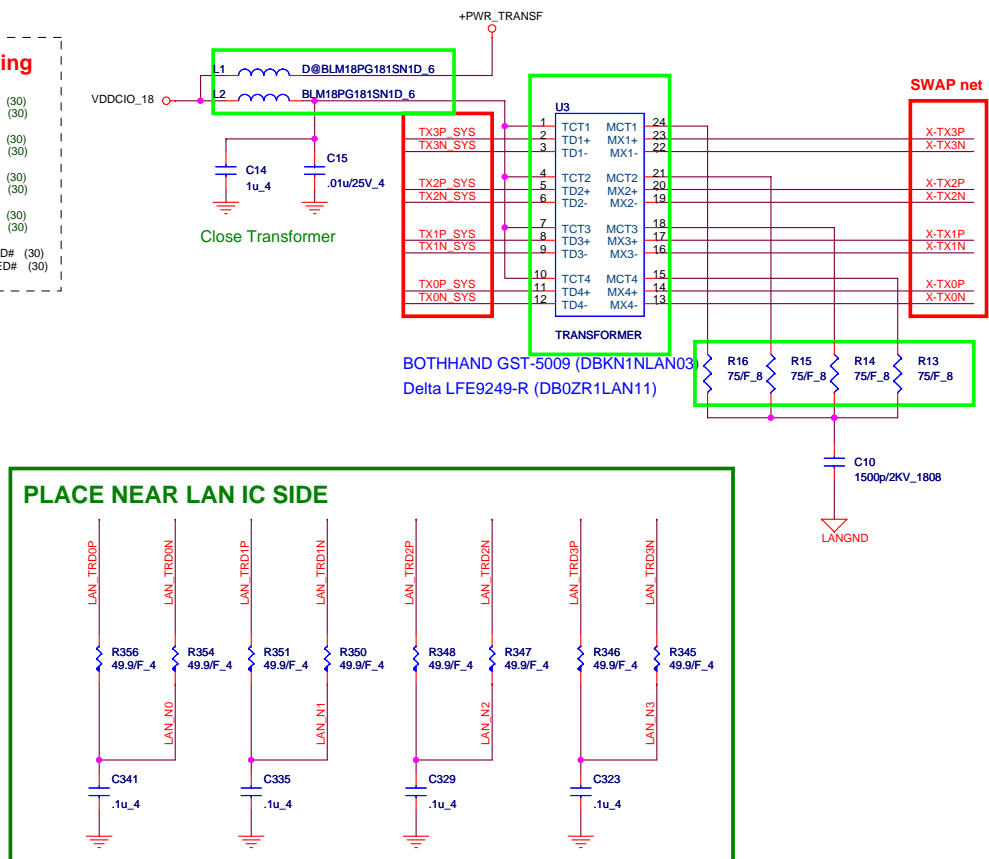
Date: Friday, June 27, 2008

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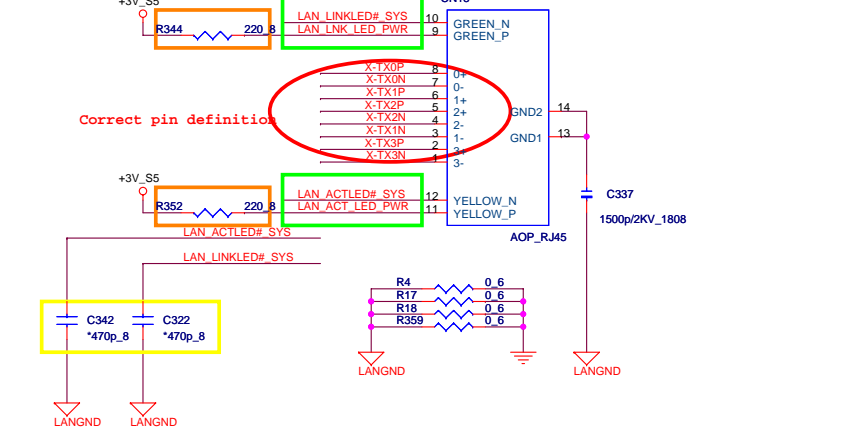
LAN SWITCH



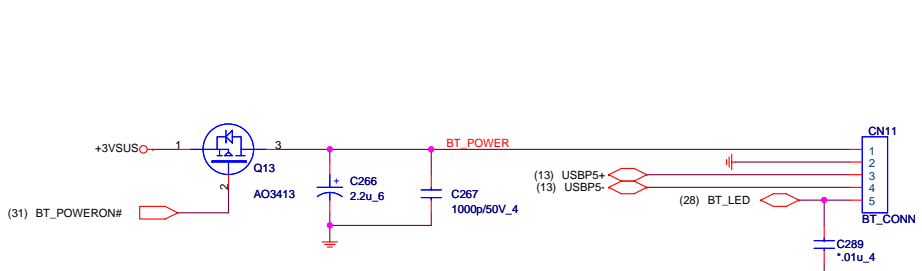
TRANSFORMER



RJ45

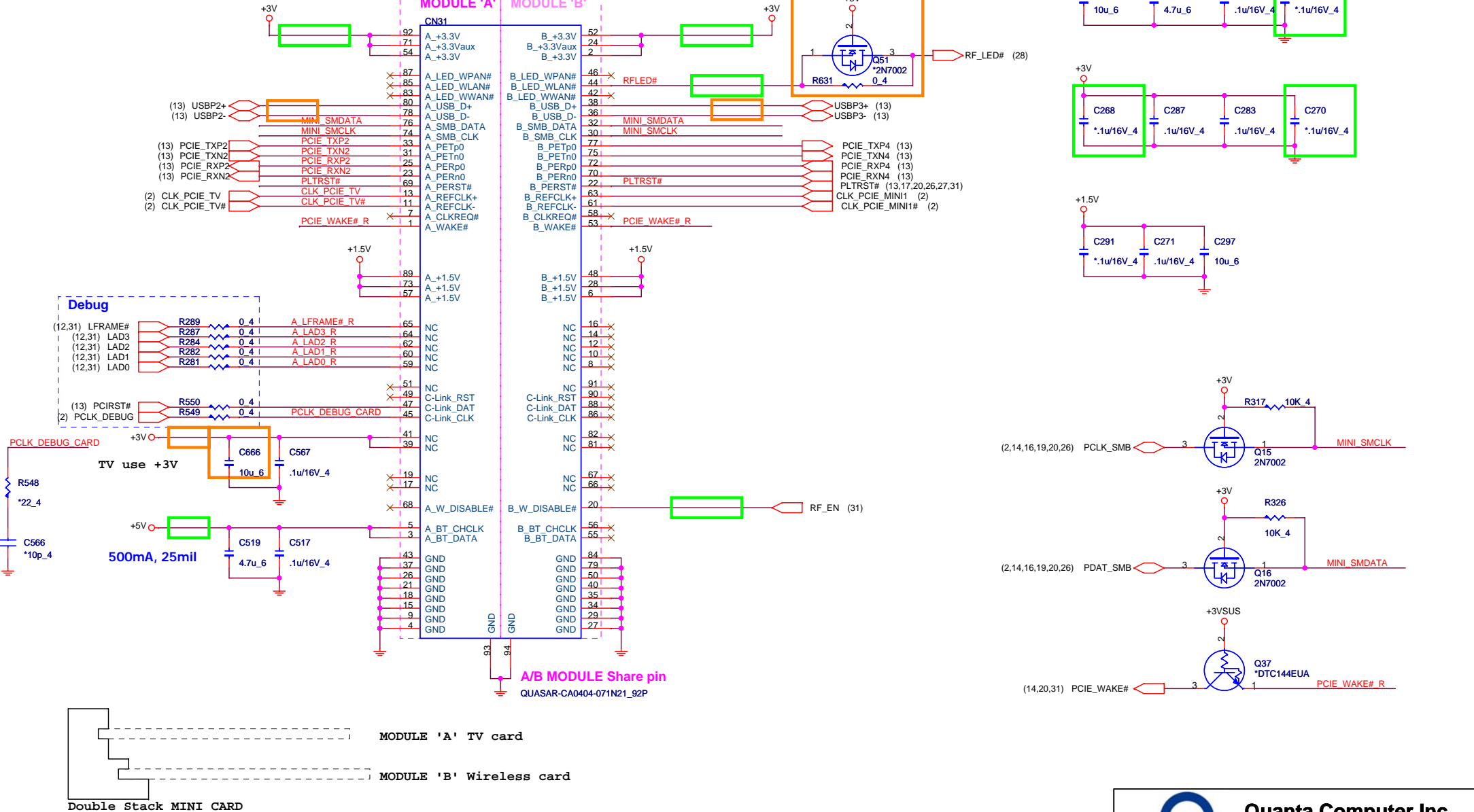


BLUETOOTH CONNECTOR



MINI-CARD

+3.3V: 1000mA
+3.3Vaux: 330mA
+1.5V: 500mA

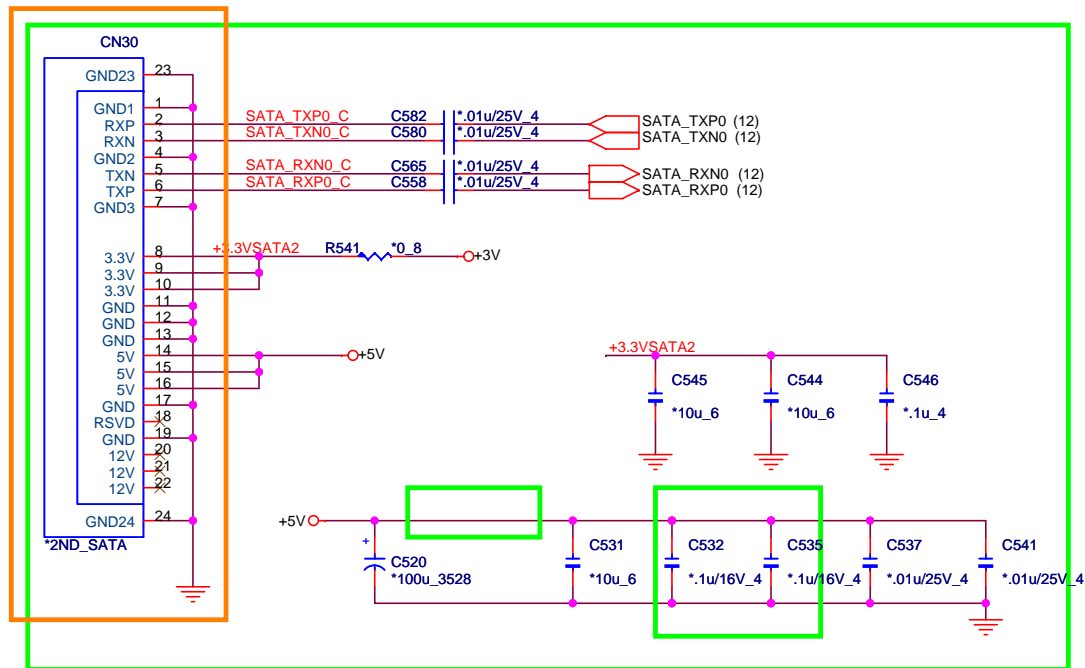


Quanta Computer Inc.

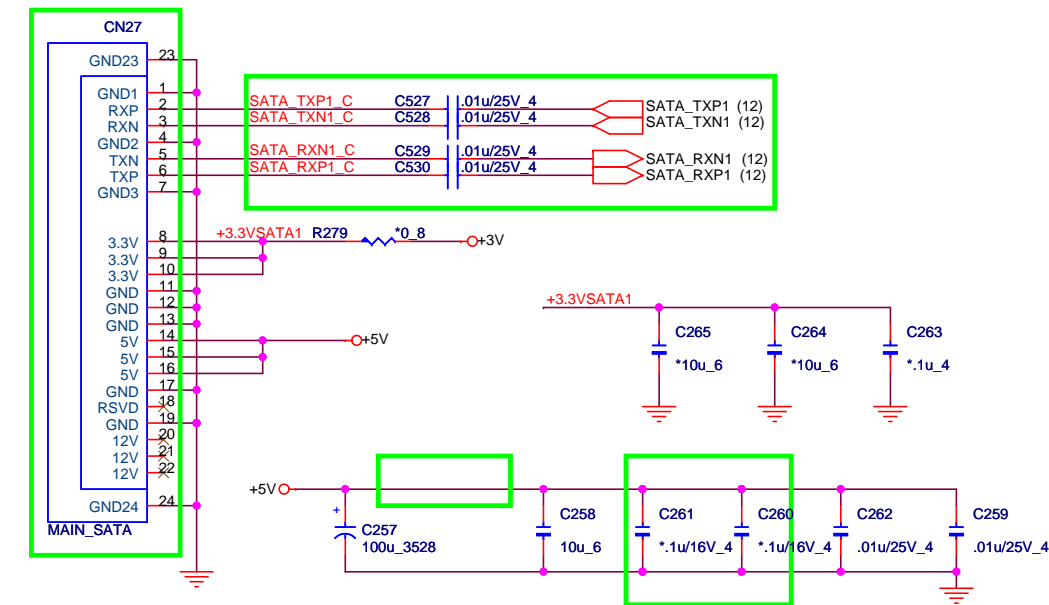
PROJECT : ZK2

Size	Document Number	Rev 3B
MINI PCI-E card/TV		
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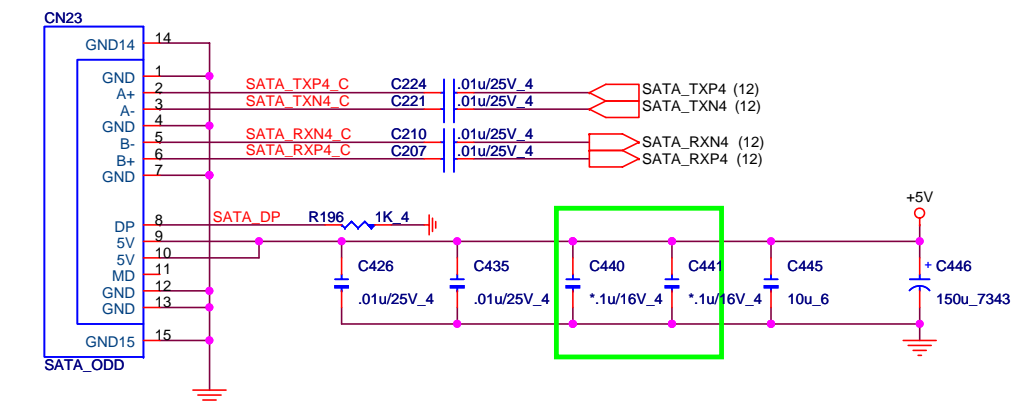
2nd SATA HDD (edge of board)



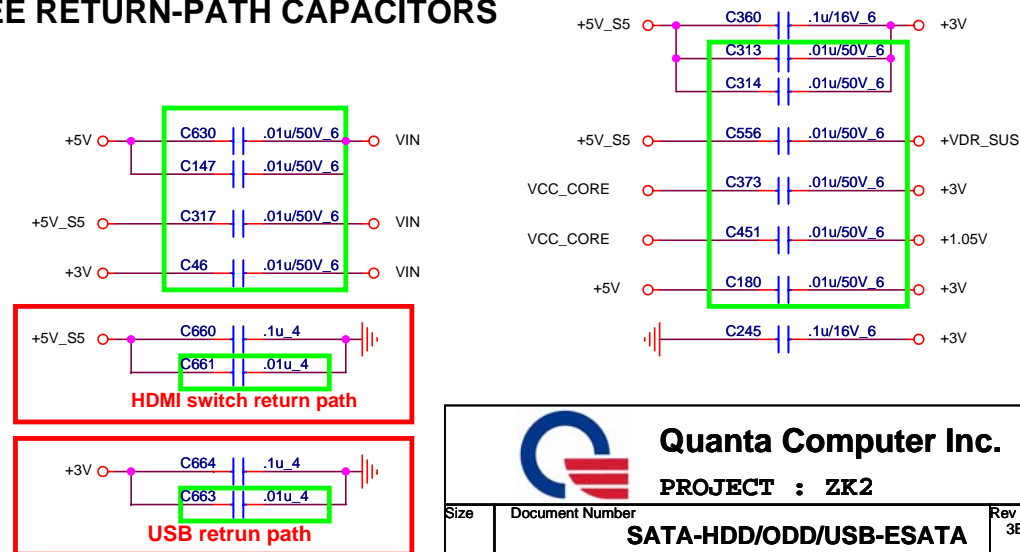
MAIN SATA HDD



ODD (SATA)



EE RETURN-PATH CAPACITORS



Quanta Computer Inc.
PROJECT : ZK2

Size	Document Number	Rev
	SATA-HDD/ODD/USB-ESATA	3B
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CODEC(ALC888S)

IV@
EV@

SPK

(25) SURR-L
(25) SURR-R

HP

(25) MONO_OUT_L
(25) SPDIF_OUT
(30) SPDIF_DOCK

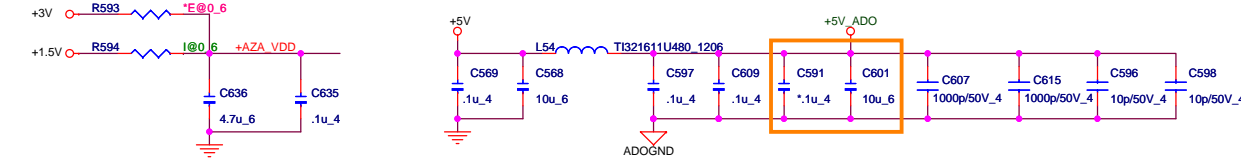
ALC888S-VC

ALC663: US0.65
ALC888S: US0.74

(18) DMIC_CLK_1
(18) DMIC0

(14) LP_ECR
(25) EAPD#

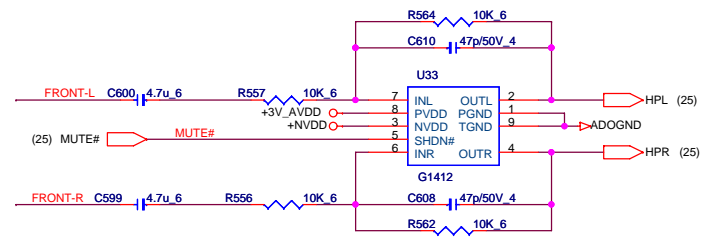
Codec Power



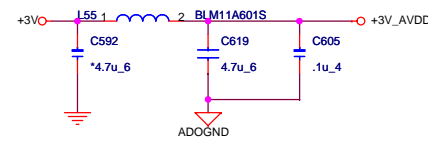
CODEC & MDC

WWW.AliSaler.Com

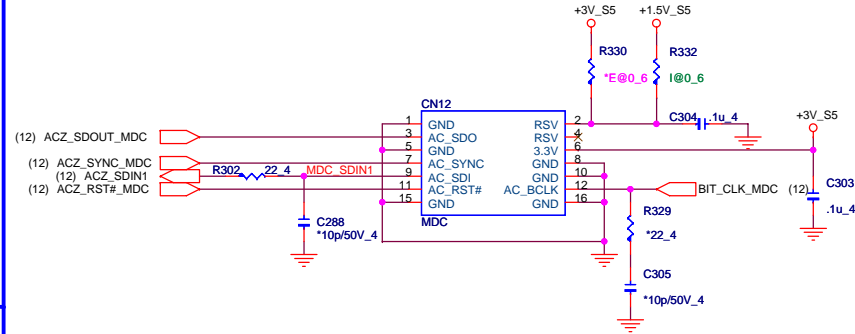
LINE-Out Amplifier



LINE-Out Amplifier Power



MDC

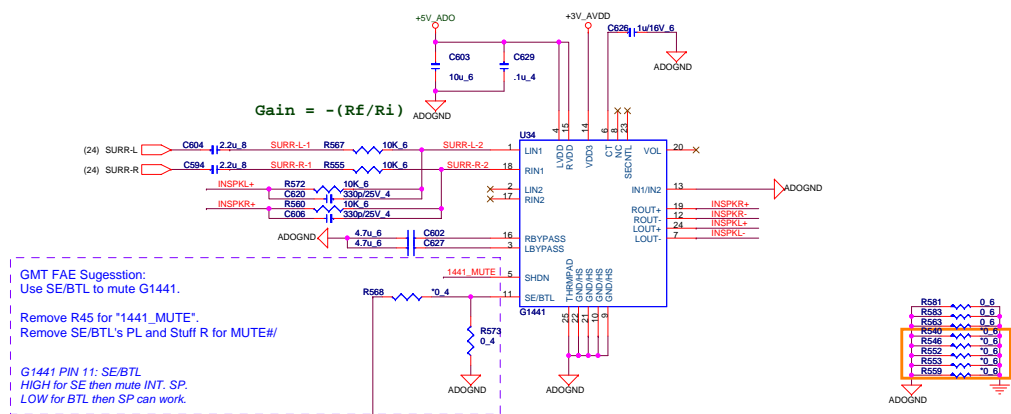


Quanta Computer Inc.
PROJECT : ZK2

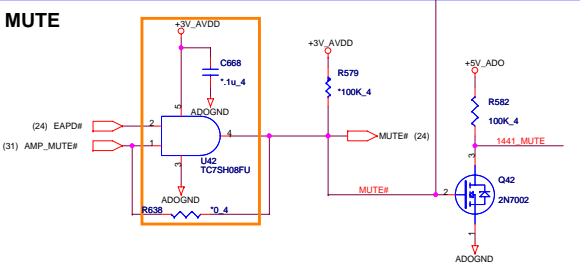
Size	Document Number	Rev
	REALTEK ALC663&888/MDC	3B

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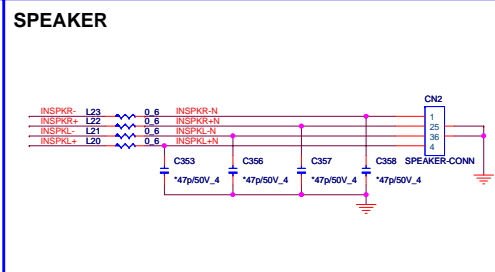
SPEAKER AMP.



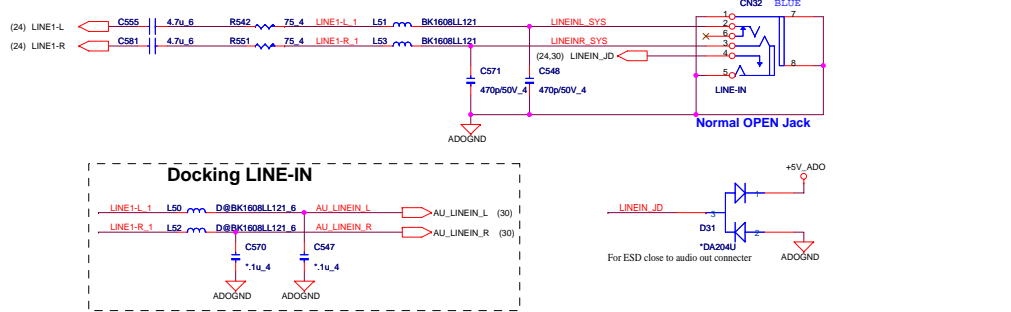
MUTE



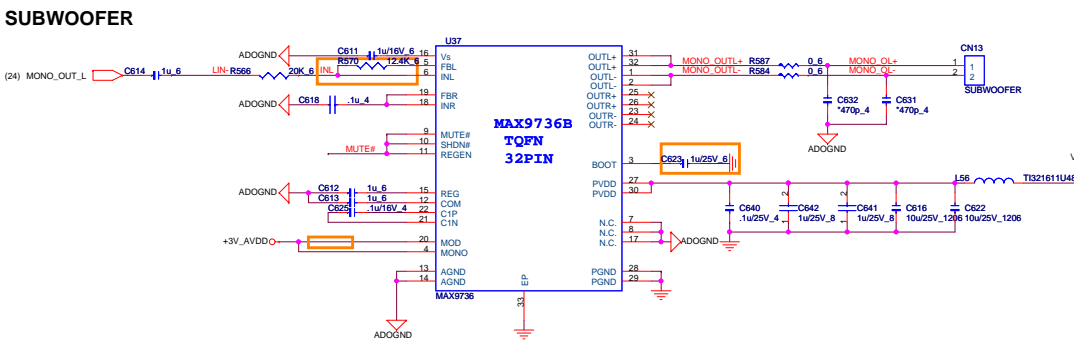
SPEAKER



LINE IN

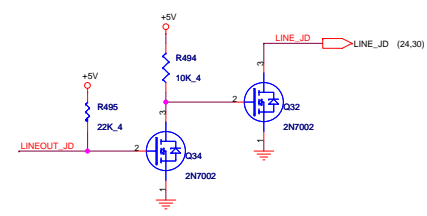
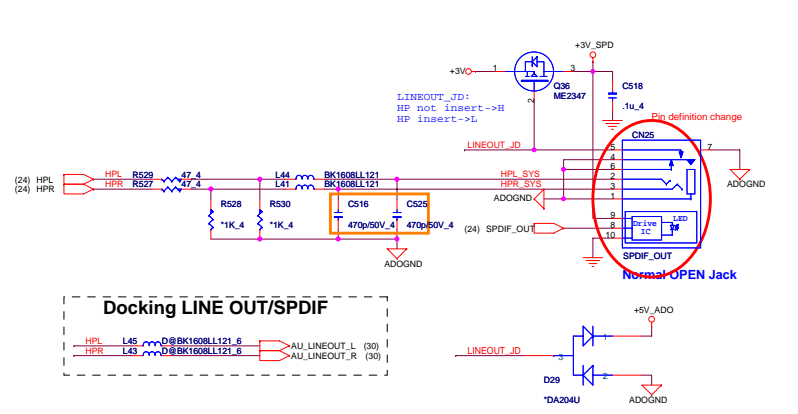


SUBWOOFER

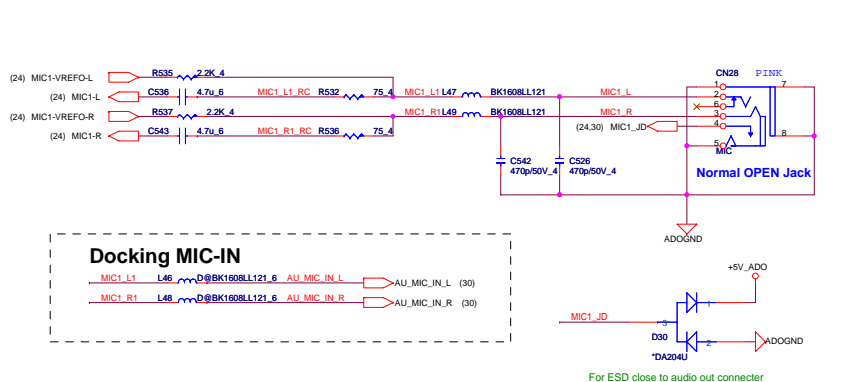


AMP& PHONE JACK & SUBWOOFER

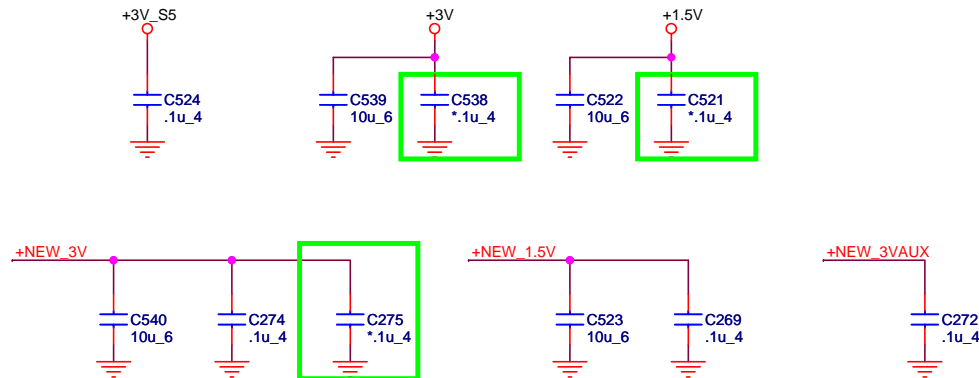
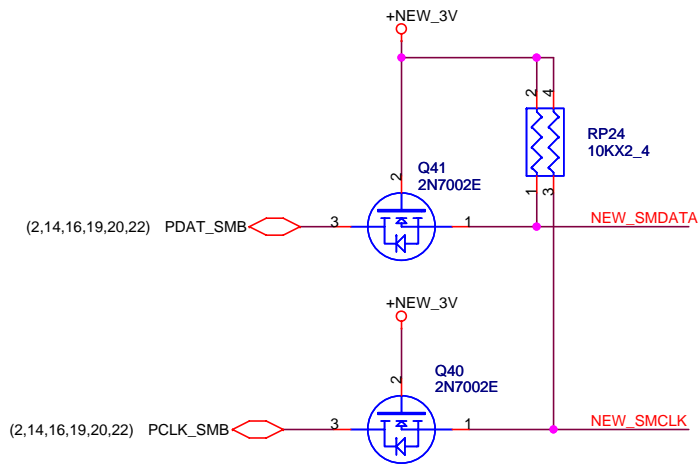
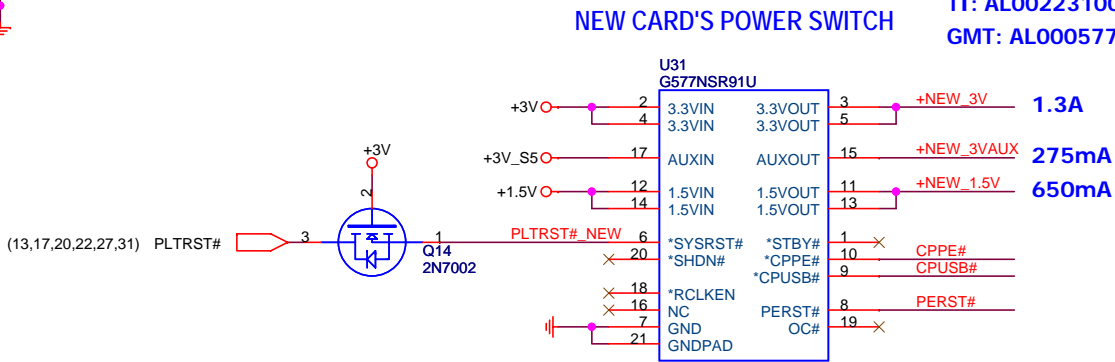
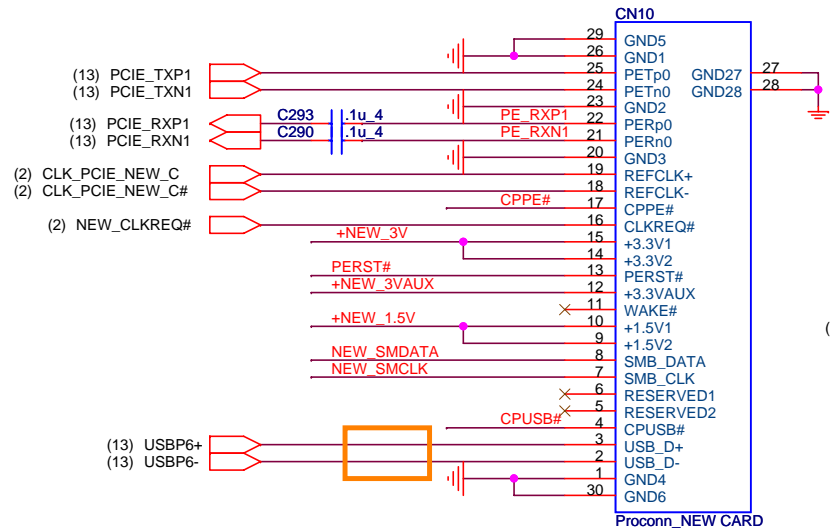
LINE-OUT/SPDIFO




MIC



NEW CARD





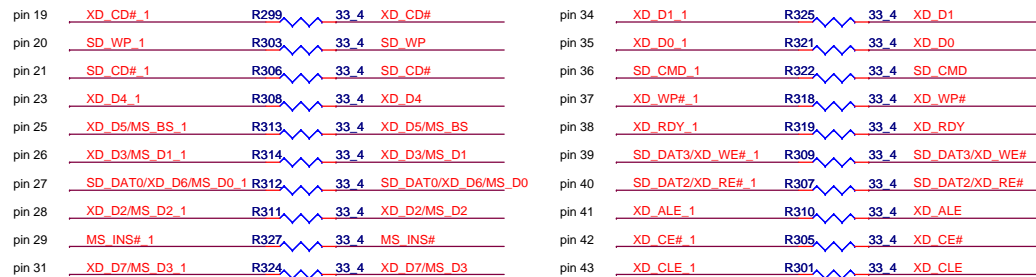
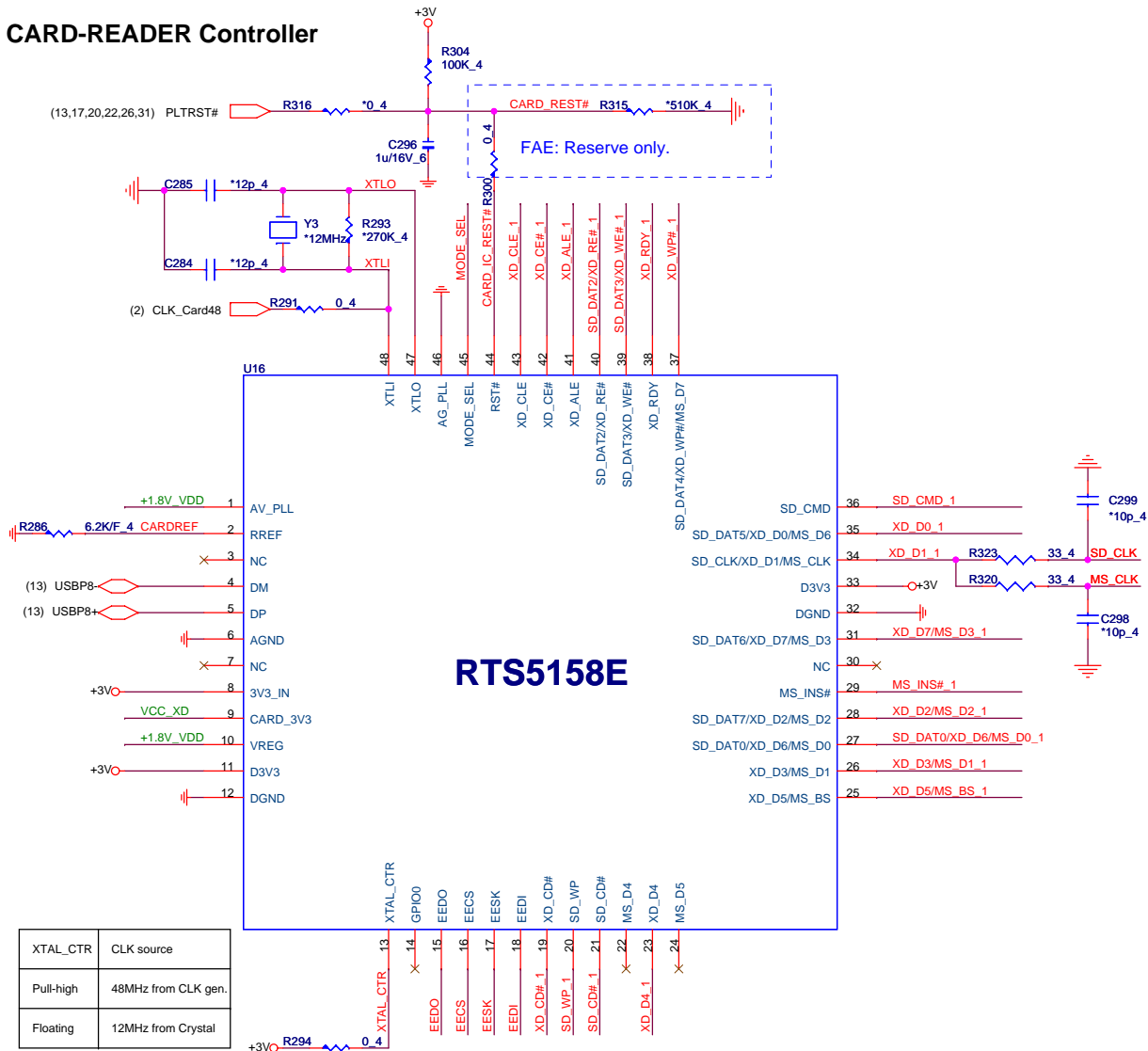
Quanta Computer Inc.

PROJECT : ZK2

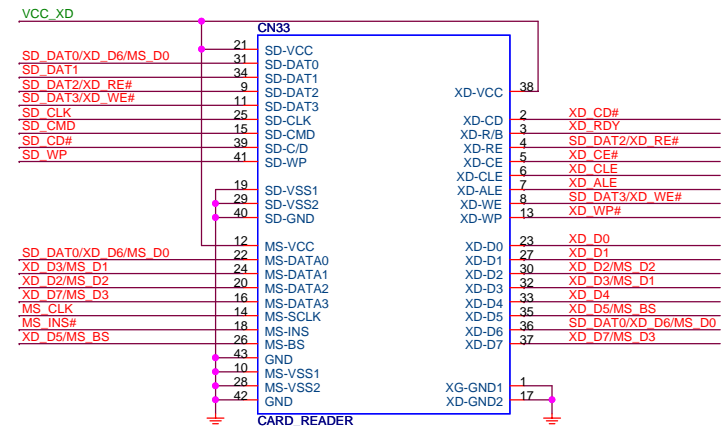
NEW CARD

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CARD-READER Controller

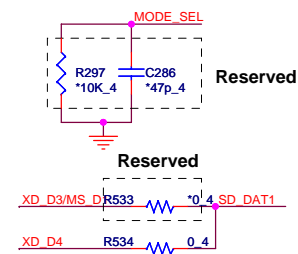


4 IN 1 CARD READER

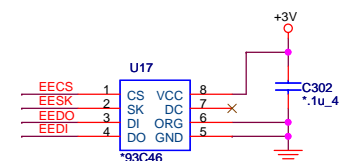


Model_Select

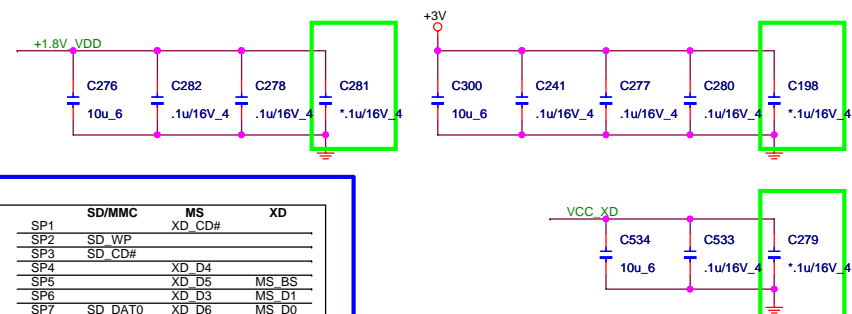
R6256/C860=NC/NC (R6258:ON)=> SD_D1 from pin23
R6256/C860=10K/47pF(R6257:ON)=>SD_D1 from pin26



EEPROM(Reserved)



Decoupling CAP



	SD/MMC	MS	XD
SP1		XD_CD#	
SP2	SD_WP		
SP3	SD_CD#		
SP4		XD_D4	
SP5		XD_D5	MS_BS
SP6		XD_D3	MS_D1
SP7	SD_DAT0	XD_D6	MS_D0
SP8	SD_DAT7	XD_D2	MS_D2
SP9		XD_D7	MS_INS#
SP10	SD_DAT6	XD_D2	MS_D3
SP11		XD_D1	
SP12	SD_DAT5	XD_D0	MS_D6
SP13	SD_DAT4	XD_WP#	MS_D7
SP14		XD_RDY	
SP15	SD_DAT3	XD_WE#	
SP16	SD_DAT2	XD_RE#	
SP17		XD_ALE	
SP18		XD_CE#	
SP19		XD_CLE	

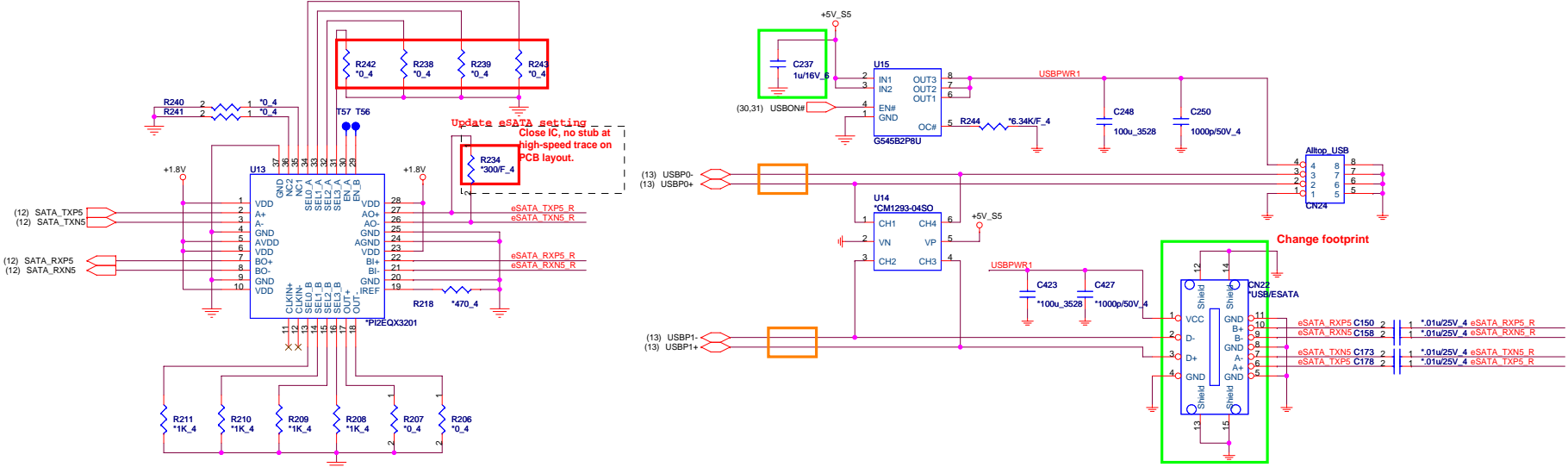


Quanta Computer Inc.

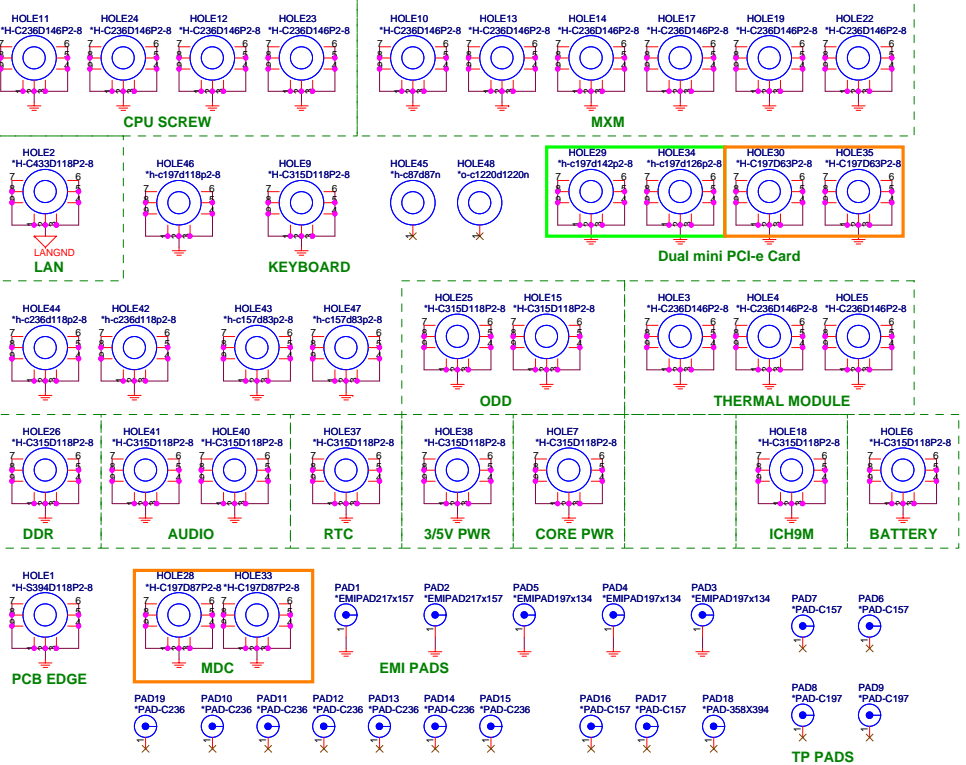
PROJECT : ZK2

CARD READER RTS5158E

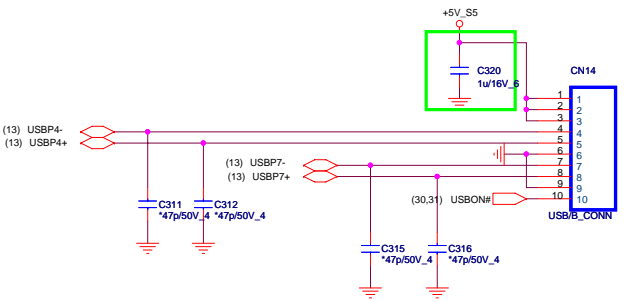
USB & ESATA



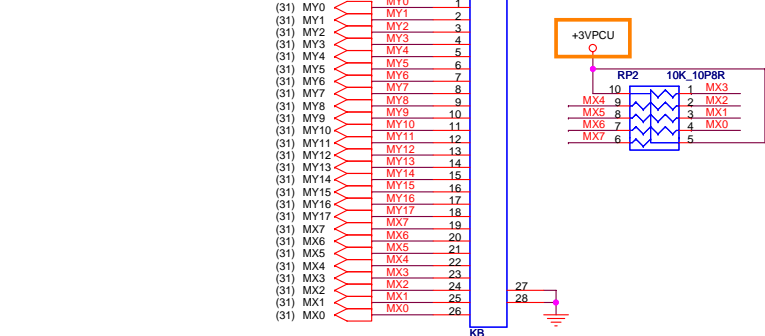
HOLES



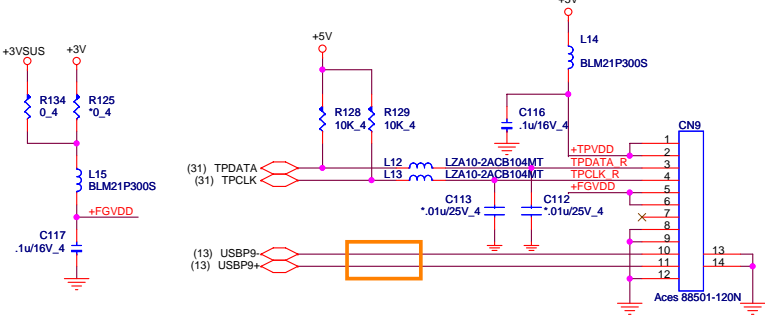
USB/B



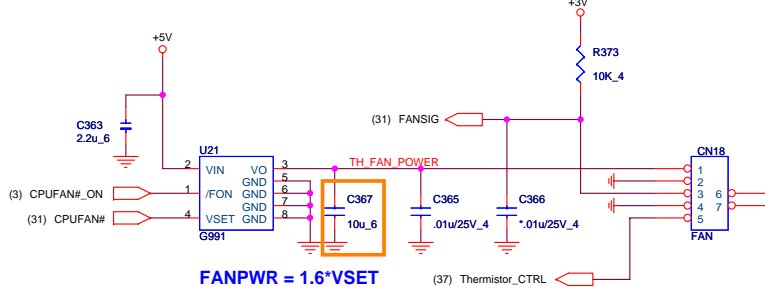
INT K/B



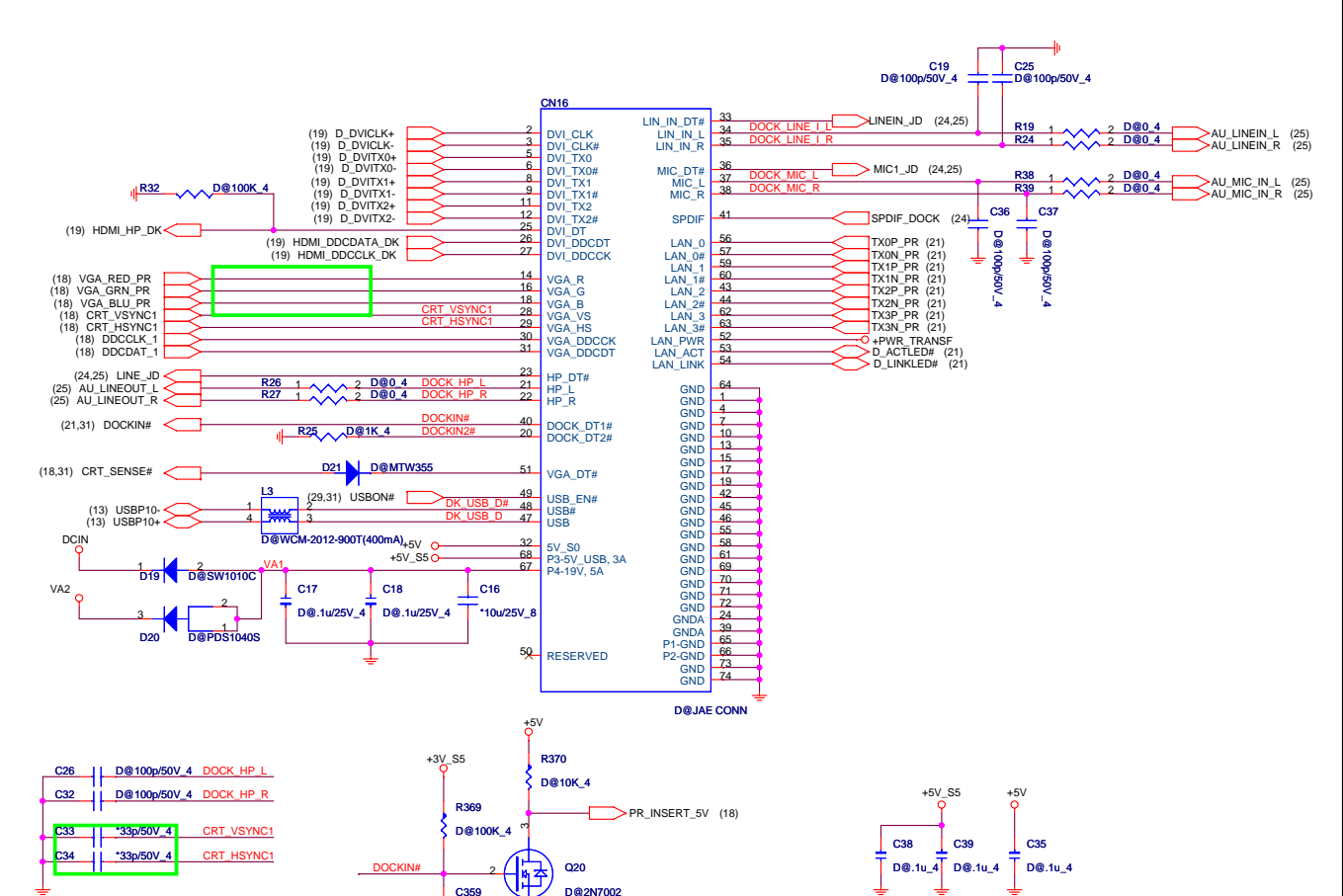
TOUCHPAD & Finger-Printer CONN.




CPU FAN



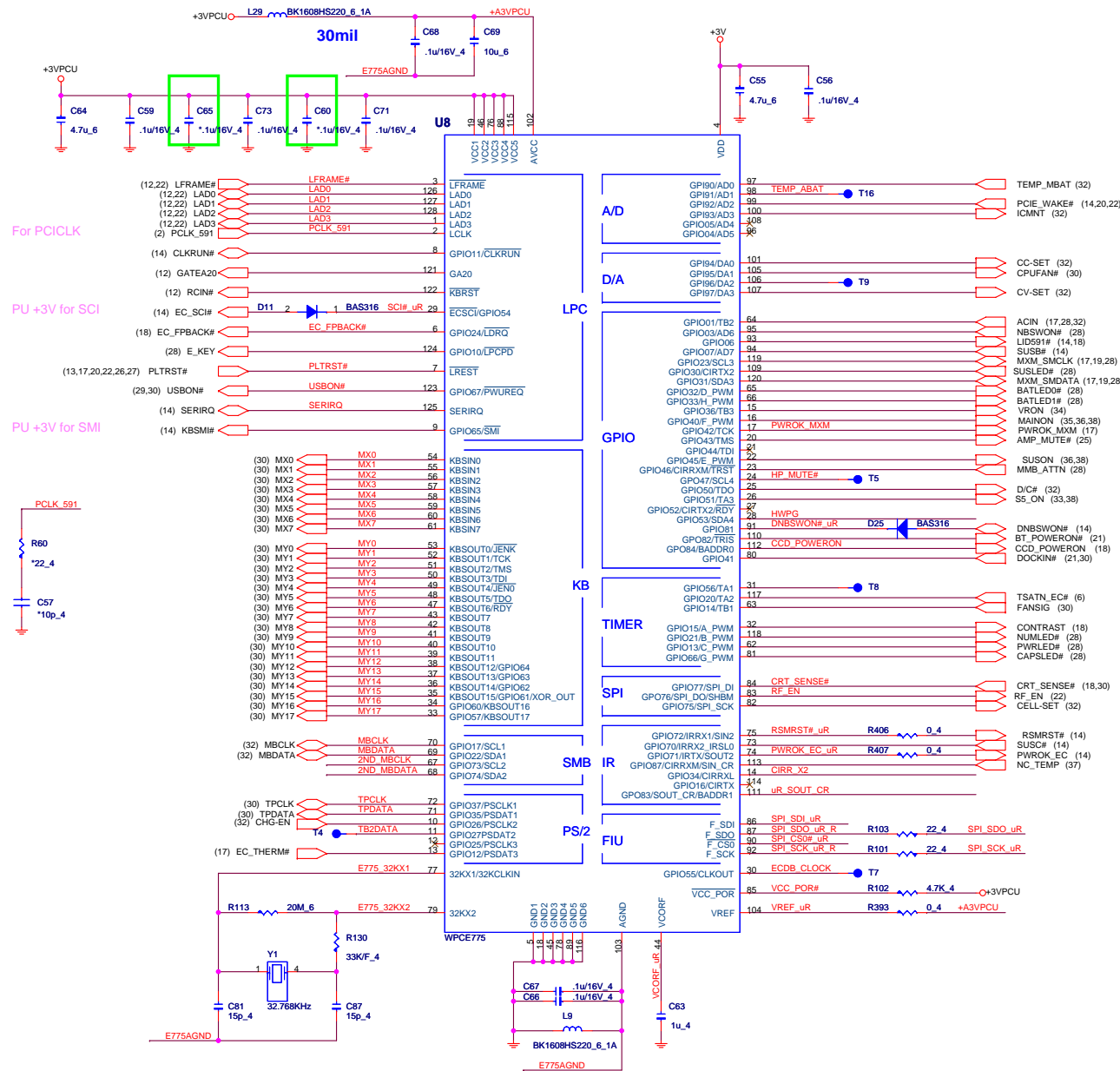
CABLE DOCK





Quanta Computer Inc.
PROJECT : ZK2

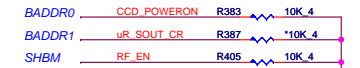
Size	Document Number	Rev
	KB/FAN/TP+FP/DOCK	3B
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I/O ADDRESS SETTING

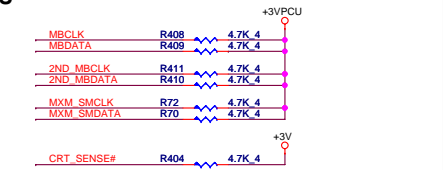
I/O Address		
BADDR1-0	Index	Data
0 0	XOR TREE TEST MODE	
0 1	CORE DEFINED	
1 0	2Eh	2Fh
1 1	164Eh	164Fh

SHBM=0: Enable shared memory with host BIOS

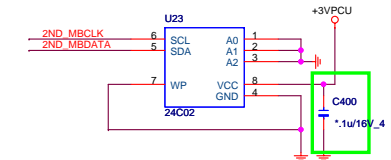


1/13 Confirm by vendor mail :
Disabled ('1') if using FW device on LPC.
Enabled ('0') if using SPI flash for both system BIOS and EC firmware

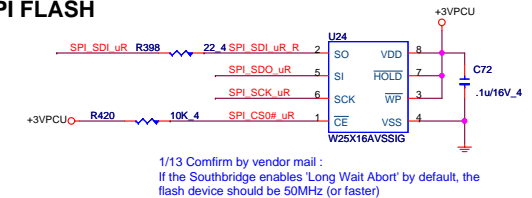
SM BUS PU



ACER ID

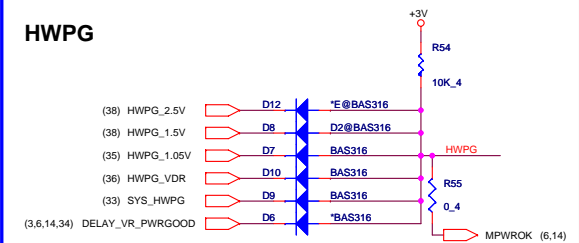


SPI FLASH

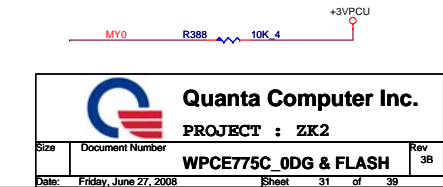


1/13 Confirm by vendor mail :
If the Southbridge enables 'Long Wait Abort' by default, the flash device should be 50MHz (or faster)

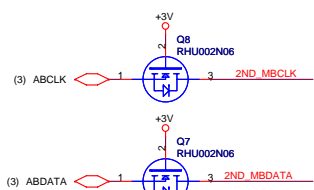
HWPG



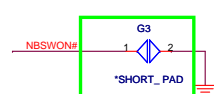
INTERNAL KEYBOARD STRIP SET



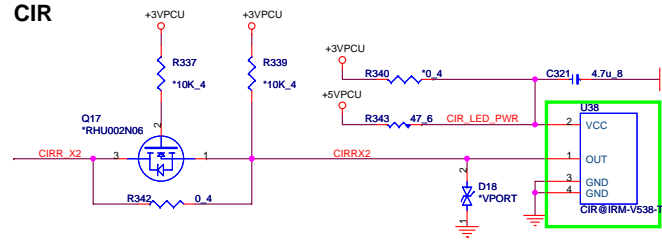
SMBus

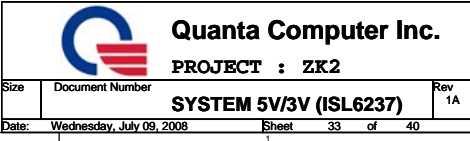


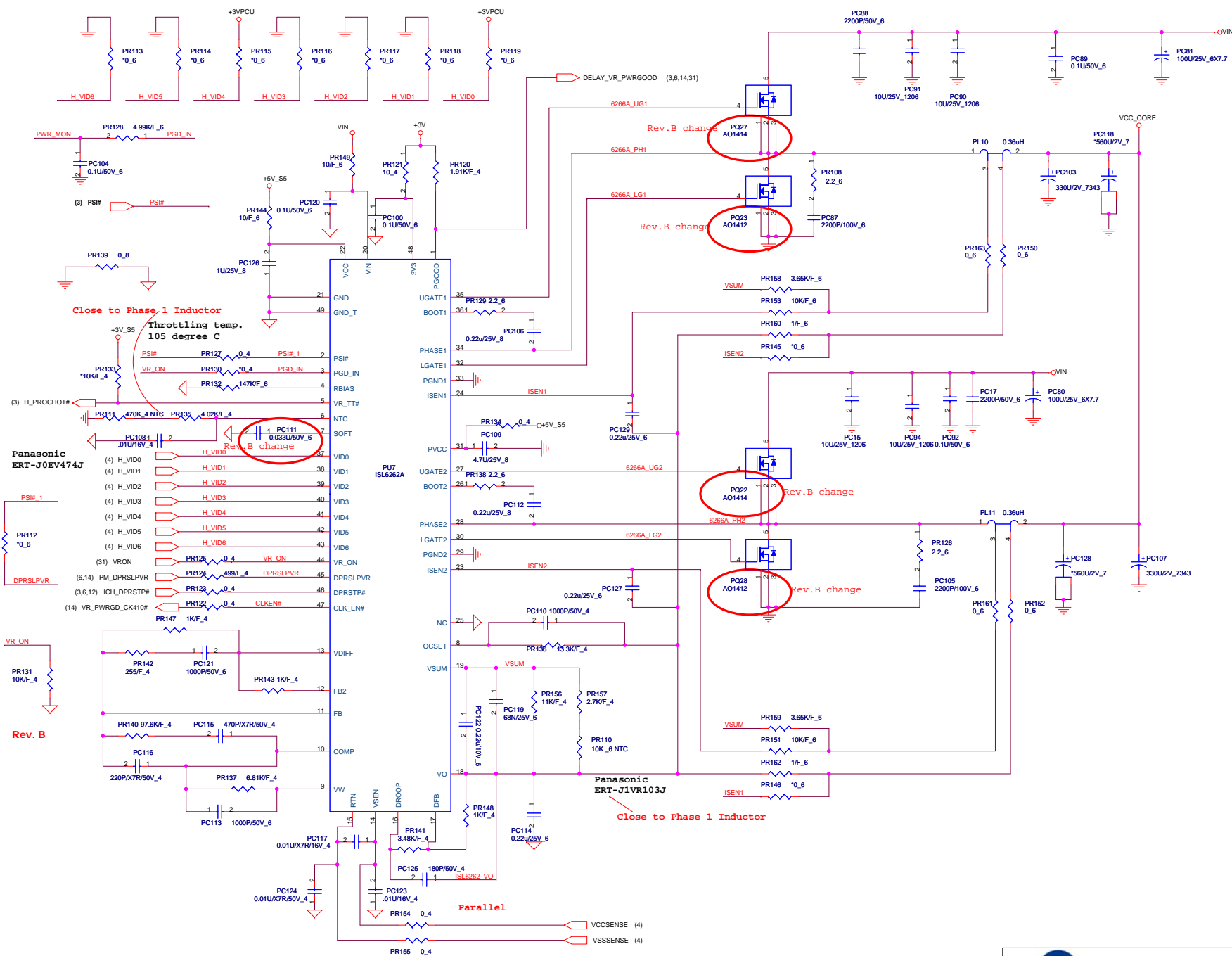
POWER-ON PAD

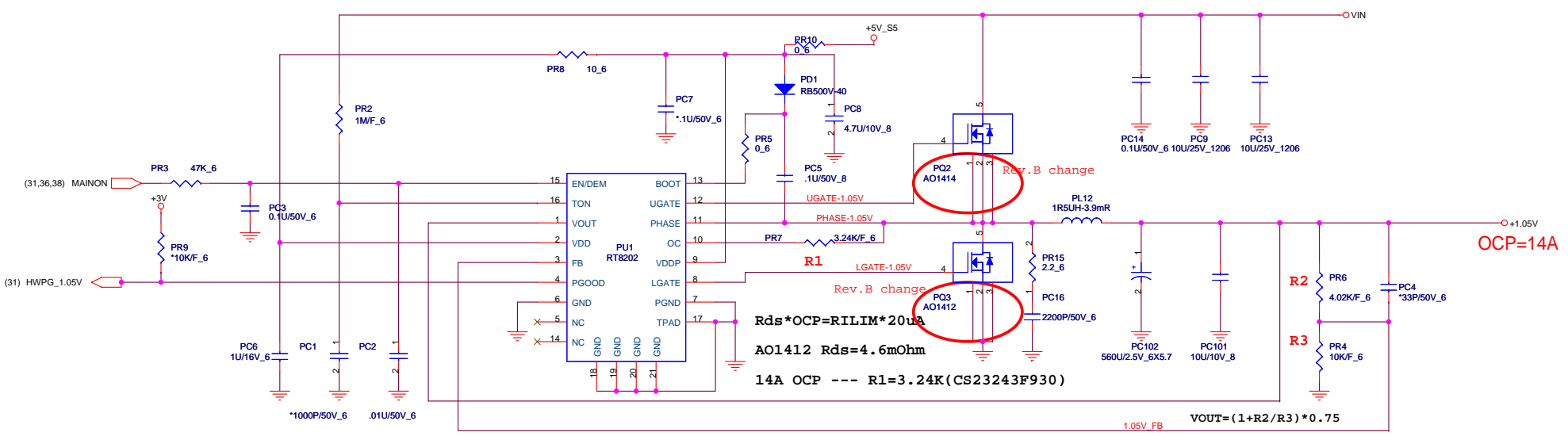


CIR

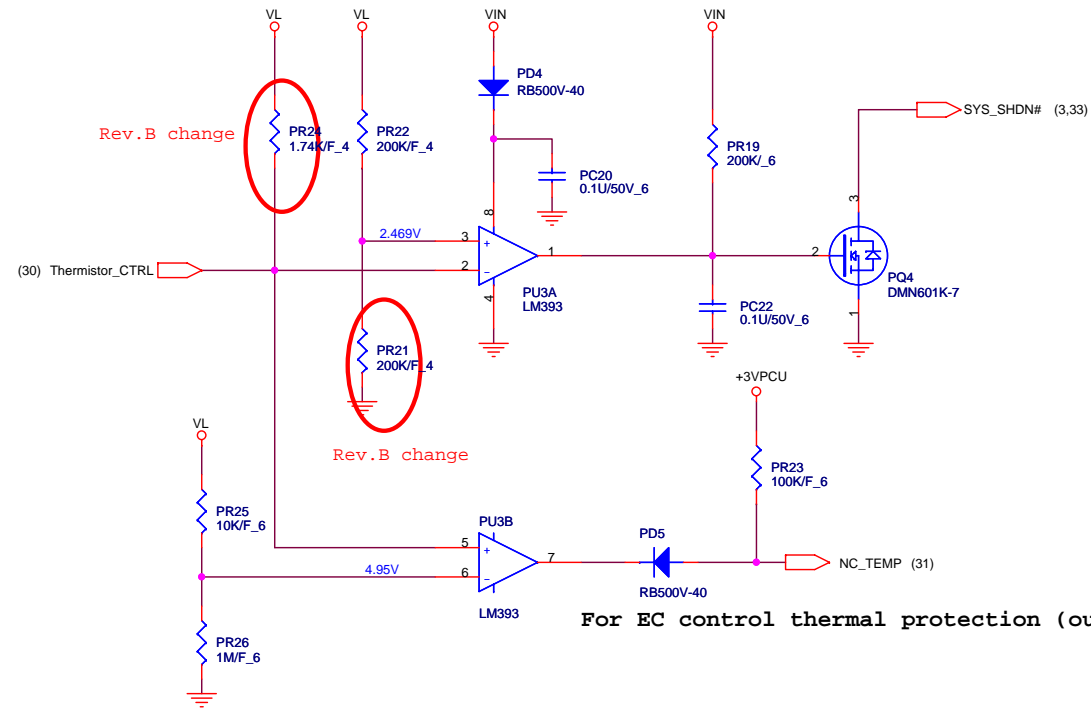








thermal protection



For EC control thermal protection (output 3.3V)



Quanta Computer Inc.

PROJECT : ZK2

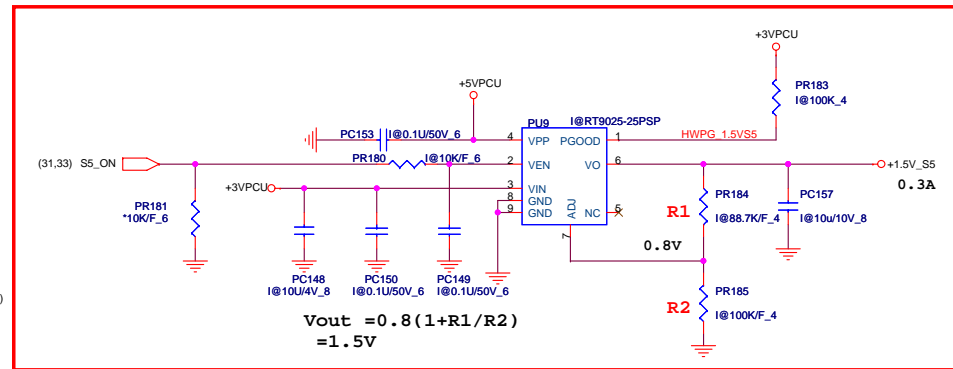
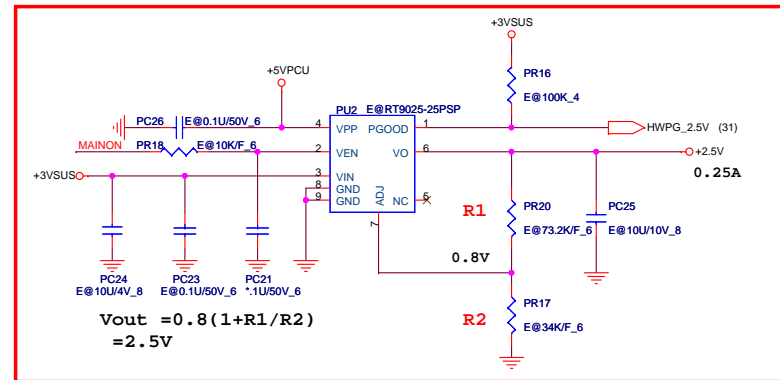
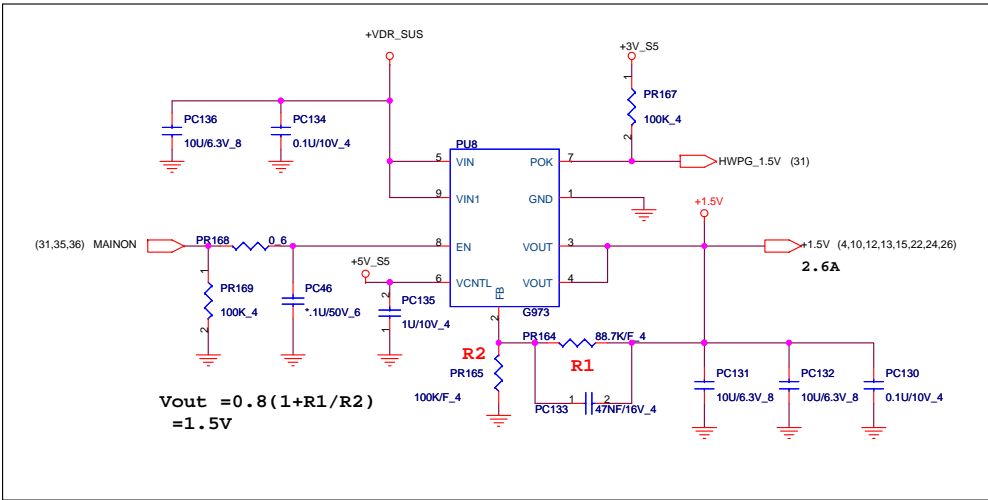
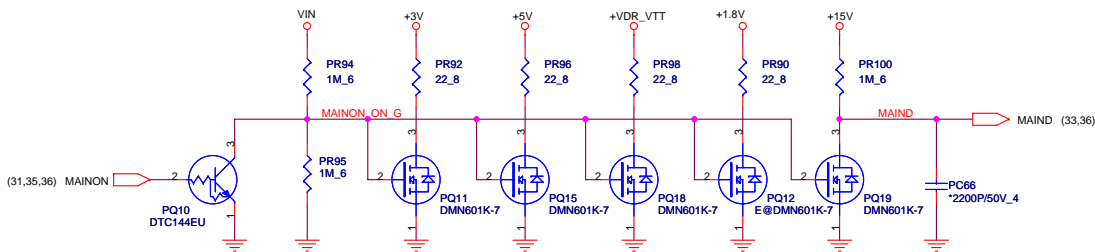
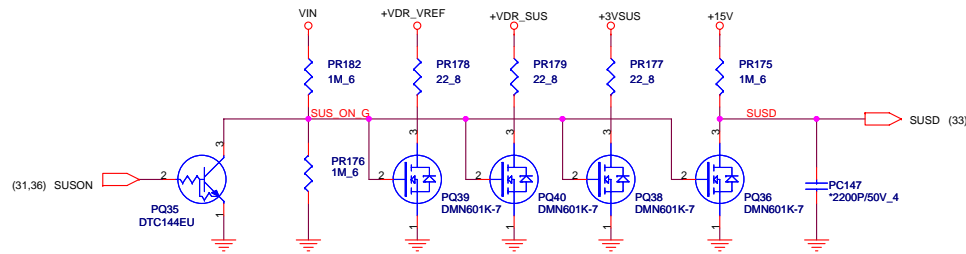
Thermal protect

Rev
1A

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Model	REV	CHANGE LIST	MODEL	ZK2	
ZK2 MB	1A	FIRST RELEASED: E200803-5424 (PCB: DAOZK2MB6A0)		FROM	To
				X	1A
				X	1A
				1A	2A
				1A	2A
				1A	2A
				1A	2A
				1A	2A
				1A	2A
				1A	2A
2A		Page10 : Correct VDD power of Northbridge to +VDD_S0H Change 32.768KHz (Y2) to normal type (R1.5) Change LCD battery connector type (CN34) to DFWD02MB311 Swap SATA port between port-1 (0DD) and port-4 (2ND HDD) Page17 : Change LCD power input capacitor (C27) to 2.2uF Change LCD power resistor (R31) to two resistors (R817/R618) for EMI Page19 : Change all HDMI switch solution to Parade (P88122), and connector type to DIP type Page20 : Correct LAN Rules (R353) to 6 pins to correct to improve performance and signal quality Correct X'tal capacitor (C351/C352) to 33pF for 25MHz Page21 : Change LAN EMI and correct R245 connector pin definition for wrong connect Page22 : Change L22 to 0ohm resistor Add two 0.1uF return-path capacitor (C660/C661) for HDMI switch Page23 : Change L6C solution for SPDIF and DMIC RMI issue Page24 : Correct SPDIF (CN65) pin definition Page28 : Change power/B power source to +3V only Page29 : Reserve +3V power source for MMIO function Modify eSATA controller (U13) swing/RQ/de-emphasis setting for signal quality, and correct eSATA connector type Move USB power switch to USB/A Page29 : Change finger-printer power source to +3VSUS Power change items Page32 : [PMS3] 6.19Kohm (CS26193P929) for MDM (90W ADP) 71.5Kohm (CS37153P917) for URM (60W ADP) Page33 : 1. Change PQ31/PQ8 from FDS8878 (BAM88780020) to A04468 (BAM44680003) 2. Change PQ30/PQ9 from FDS6690A8 (BAM66900022) to A04712 (BAM47120000) 3. Change PQ32/PQ33 from PDC6553 (BAM65300003) to A06402A (BAM64020000) 4. Change PR61 from 150K/F_4 (CS41502PB18) to 150K/F_4 (CS41502PB10) 5. Change PR71 from 178K/F_6 (CS41783P918) to 237K/F_6 (CS42373P911) 6. Change PR65 from 196K/F_6 (CS41963P916) to 249K/F_6 (CS42493P914) Page34 : 1. Change PQ27/PQ22 from TPCAB023-H (BAM80230000) to A01414 (BAM14140001) 2. Change PQ28/PQ23 from TPCAB019-H (BAM80190000) to A01412 (BAM14120000) 3. Change PQ11 from 0.0220/50V_6 (CH3326K1901) to 0.0330/50V_6 (CH3336J1900) Page35 : 1. Change PQ2 from TPCAB023-H (BAM80230000) to A01414 (BAM14140001) 2. Change PQ3 from TPCAB019-H (BAM80190000) to A01412 (BAM14120000) Page36 : 1. Change PQ41 from TPCAB023-H (BAM80230000) to A01414 (BAM14140001) 2. Change PQ37 from TPCAB019-H (BAM80190000) to A01412 (BAM14120000) 3. Change PR82 from 5.62K/F_6 (CS25623P914) to 4.75K/F_6 (CS24753P919) Page37 : 1. Change PR21 from 196K/F_4 (CS41962PB01) to 200K/F_4 (CS42002PB12) 2. Change PR24 from 1.43K/F_4 (CS21432PB00) to 1.74K/F_4 (CS21742PB00)			
				2A	3A
				2A	3A
				2A	3A
				2A	3A
				2A	3A
				2A	3A
				2A	3A
				2A	3A
				2A	3A
3A		Page2 : no mount 0.1uF (C475/C492/C471) Page3 : no mount 0.1uF (C151) Page4 : remove 0 ohm (R450/R390/R402/R159), and connect them directly Page12 : remove 0 ohm (R498/R249/R487), and connect them directly Swap Main HDD to port-0, and 2nd HDD to port-4 Page13 : remove 0 ohm (R198), and connect them directly Swap USB port2 to external USB, and port-7 to Cardreader Page14 : remove 0 ohm (R186/R185/R466/R235/R506), and connect them directly. no mount 0.1uF (C170/C448) Page16 : no mount 0.1uF (C101/C552) Page17 : reserve 0 ohm (R626) from MDM to EC (EC_THERM#) no mount 0.1uF (C489) Page18 : no mount Q21/Q24 and bypass from 0ohm (R378/R381), pull-up 2K ohm to +3V for MDM sku Change L67/7/8 to BLM18BA4708N1D Change U4 to A2004280001 (AA74280-4) part Remove 0 ohm (R22), and connect directly Change CN3 to DFWW40MR000 for SMT request Change R42 from 330 ohm to 180 ohm (CN11802PB12) Page19 : Use 100 ohm (R419/R620/R621/R622) and 1uF (C556/C657/C658/C659) for HDMI EMI request Reserve C662/Q43/Q44/R119/R126, and bypass 0ohm (R627/R628) Page20 : remove 0ohm (R5/R9/R357) and connect directly Page21 : Change L1/L2 (BLM18BA4708N1D) to increase current rating Change transformer to GST-5009 Change R13-R16 from 75ohm 0402 to 0805 size no mount 0.1uF (C350) Swap LAN LED color connect (green: linking/orange:active) Page22 : Remove R296/R292/R328/L42/R298 and connect directly no mount 0.1uF (C247/C270/C268) Page23 : Change main (CN27) and 2nd (CN30) HDD footprint for M/B request no mount 0.1uF (C532/C535/C260/C261/C440/C441) Change 0.1uF to 0.04uF (C630/C347/C317/C46/C661/C663/C313/C314/C556/C373/C451/C180) Page24 : remove 0ohm (R574) and connect directly Page25 : no mount 0.1uF (C281/C198/C279) Page26 : Add AC-IN LED-on function (C48/Q50) Add PWMLED/SUSLED function on Power/B (Q47/Q49/R624/R625) Change R47/R49 from 0ohm to 100ohm for synaptic MMB Page29 : Change L27, L28, L29, L30, L31, L32, L33, L34, L35, L36, L37, L38, L39, L40, L41, L42, L43, L44, L45, L46, L47, L48, L49, L50, L51, L52, L53, L54, L55, L56, L57, L58, L59, L60, L61, L62, L63, L64, L65, L66, L67, L68, L69, L70, L71, L72, L73, L74, L75, L76, L77, L78, L79, L80, L81, L82, L83, L84, L85, L86, L87, L88, L89, L90, L91, L92, L93, L94, L95, L96, L97, L98, L99, L100, L101, L102, L103, L104, L105, L106, L107, L108, L109, L110, L111, L112, L113, L114, L115, L116, L117, L118, L119, L120, L121, L122, L123, L124, L125, L126, L127, L128, L129, L130, L131, L132, L133, L134, L135, L136, L137, L138, L139, L140, L141, L142, L143, L144, L145, L146, L147, L148, L149, L150, L151, L152, L153, L154, L155, L156, L157, L158, L159, L160, L161, L162, L163, L164, L165, L166, L167, L168, L169, L170, L171, L172, L173, L174, L175, L176, L177, L178, L179, L180, L181, L182, L183, L184, L185, L186, L187, L188, L189, L190, L191, L192, L193, L194, L195, L196, L197, L198, L199, L200, L201, L202, L203, L204, L205, L206, L207, L208, L209, L210, L211, L212, L213, L214, L215, L216, L217, L218, L219, L220, L221, L222, L223, L224, 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